DIVISION OF STRUCTURES AND ENGINEERING SERVICES

TRANSPORTATION LABORATORY

RESEARCH REPORT

TRAFFIC RESPONSIVE RAMP CONTROL THROUGH THE USE OF MICROCOMPUTER

FINAL REPORT

FHWA-CA-TL-1639-77-04

FEBRUARY 1977

Prepared in Cooperation with the U.S. Department of Transportation,

Federal Highway Administration

Caltrans

CALIFORNIA DEPARTMENT OF TRANSPORTATION

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16. ABSTRACT

This research was involved in the investigation, development, and implementation of ramp control hardware and software through the use of microcomputer. A prototype controller consisting of a 4-bit Intel microprocessor and 2096 x 8 bit of programmable read-only-memory was developed for exploratory study. It was concluded that the second generation N-MOS microprocessors have superior instruction power and hardware capabilities than their P-MOS predecessors. The Type 140 Controller design specification was prepared under this research. The first 200 units of the Type 140 Controller, have been purchased for implementation. Programs for traffic responsive ramp control have been developed under this research to be implemented with the Type 140 Controller.

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STATE OF CALIFORNIA
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DIVISION OF STRUCTURES & ENGINEERING SERVICES
OFFICE OF TRANSPORTATION LABORATORY

December 1976

FHWA No. C-1-20
TL No. 631639

Mr. C. E. Forbes
Chief Engineer

Dear Sir:

I have approved and now submit for your information this final research project report titled:

TRAFFIC RESPONSIVE RAMP CONTROL THROUGH
THE USE OF MICROCOMPUTER

Study made by . . . . . .General Services Branch

Under the Supervision of . . . . . .W. H. Ames, P. E.

Principal Investigator . . . . . .R. L. Donner, P. E.

Co-Investigator. . . . . .B. C. Fong, P. E.

Report Prepared by . . . . . .B. C. Fong, P. E.

Very truly yours,

George A. Hill

GEORGE A. HILL
Chief, Office of Transportation Laboratory

BCF:bjs
Attachment

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ACKNOWLEDGEMENTS

This work was accomplished in cooperation with the United States Department of Transportation, Federal Highway Administration, work program HPR-PR-1(11), Part 2 Research as Item C-1-20, titled "Traffic Responsive Ramp Control Through the Use of Microcomputers".

The contents of this report reflect the views of the Transportation Laboratory which is responsible for the facts and the accuracy of the data presented herein. The contents do not necessarily reflect the official views or policies of the State of California or the Federal Highway Administration. This report does not constitute a standard, specification, or regulation.

The investigators wish to express their appreciation to L. G. Kubel, the traffic coordinator and the staff at Headquarters Traffic Branch for their major contribution in developing and implementating the 140 ramp controller and to C. W. Wasser for his effort in the development of the ramp control strategies.

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I. INTRODUCTION

As the nation's interstate freeway system approaches completion, more emphasis is now being directed toward improved operation of existing freeways. Ramp control has been used with various degrees of effectiveness in the improvement of traffic flow on freeways during peak traffic periods.

Ramp control methods currently in operation include ramp closure, fixed-time metering, and real-time traffic responsive metering.

The fixed-time metering method usually employs the use of traffic signals and a controller at the on-ramp to activate a metering rate preset according to the time-of-day. The preset metering rates are calculated from historical upstream demand and downstream capacity data. It does not cycle or respond to real-time traffic conditions.

The fixed-time metering method has achieved considerable improvement, however, they are unable to adjust to real-time traffic patterns. Traffic reponsive metering has experienced significant success in Los Angeles, Chicago, Detroit, Houston, Dallas and other major cities. Installations at these locations involves the use of a large scale process computer to monitor the traffic condition along a stretch of freeway consisting of many ramps and to adjust the individual metering rate accordingly. Although the large scale computer systems have the capability for real-time traffic controls, they are not cost effective for isolated or widely separated areas where only a few ramps are involved. The advent of microcomputer, or computer on chips, has enabled many new applications for industries and in the field of transportation. As this market becomes more competitive, their prices are also becoming more attractive. Microcomputers can now replace minicomputers in most automatic control applications with significant reductions in cost and physical size.

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The objective of this project was to evaluate the use of a microcomputer as a traffic responsive ramp controller. This controller would be used as a stand alone controller and/or as a local processor for a multi-level corridor control system. In general, this controller would have the capability to perform the following functions:

1. Monitor the vehicle sensors on the main lane and on-ramp roadways and compute their occupancies and vehicular counts over the past one minute period.

2. Actuate traffic signal heads at the metering rates dictated by their respective real-time occupancies and/or by a historical file referenced to a seven-day clock.

3. When it is interconnected as a local processor for a multi-level system, it would only monitor and compute local traffic data, and yield control jurisdiction to the central computer for corridor controls.

However, in the event of a failure in the central computer or in the communication link, the controller would take over control operation in either fixed-time or local traffic responsive modes.

4. All functions and metering rates would be controlled by software programs so that they could easily be modified to reflect changes in control strategy.

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II. CONCLUSIONS

Based on the findings of this research project, a design specification has been developed for a Type 140 Controller. Two hundred of the controller units have been purchased in accordance with the State's design specification. The attractive features found in the Type 140 Controller include the following:

1. Flexibility -- The ramp control software can be changed easily to reflect changes in control philosophy or in future traffic patterns. This is usually a costly and difficult task for the dedicated fixed logic type controllers.

2. Cost -- The unit cost of the Type 140 Controller in 1976 was approximately $1,350, or $3,600 including cabinet, modem, and detector amplifiers. This is substantially lower than a controller which employs a minicomputer, and yet it does not sacrifice any essential feature needed for general traffic controls.

3. Environmental -- The Type 140 Controller has an operational temperature range of -18°C to 60°C. Unlike the minicomputer controller it can be operated in any geographical location in California without the use of air conditioning.

4. Physical Size -- The physical size of the Type 140 Controller is relatively smaller than controllers employing minicomputers. This is because of the use of the much smaller microprocessor and memory chips, smaller DC power supply, and the elimination of air conditioning.

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5. Operation and Maintenance -- As part of a multi-level system, having an "intelligent" controller at each ramp will significantly increase the reliability of the system. Also, having the local controllers processing the local traffic data will allow the central computer more time for corridor analysis and incident detection.

The ramp control program developed under this research project for the Type 140 Controller is capable of fixed-time or traffic responsive ramp control for local or multi-level ramp control. Details of the control algorithm, flow charts, and program listings are described in the Discussion section of this report. This program contains all the essential provisions needed to meter any ramp location by simply entering the appropriate metering parameters into the designated locations in the randam access memory.

Some of the benefits and advantages to be gained by the public from this research and from properly implementing the Type 140 Controller include:

1. Reduction of mental strain on the motorist.

2. Reduction of rear end type accidents on freeways.

3. Reduction of overall travel time, including motorists using the freeway and those choosing to use alternate routes.

4. Increased efficiency of freeways with a corresponding increase of throughput in total vehicle miles.

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5. Reduction of fuel consumption and air pollution by minimizing the congested stop and go traffic pattern.

6. Encouraging the public to accept and utilize car pools and bus ridership with the preferential access provisions.

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III. RECOMMENDATIONS

1. The Type 140 Controller hardware and software provides a powerful tool to control ramp traffic. However, the ultimate effectiveness in reducing congestion and achieving the optimum traffic flows lies with the control parameters which the traffic engineers enter into the controllers. Therefore, it is recommended that traffic engineers carefully monitor the traffic behavior throughout the initial metering period and adjust the control parameters as necessary until optimum traffic flows are achieved.

2. It is recommended that further research be done in data communications in order to carry out the plan of interconnecting the ramp controllers into multi-level control systems.

3. Guidelines should be established for the design and selection of the most cost effective communication components and transmission lines.

4. Testing and maintenance procedures should be setup to improve the reliabilities of existing and new equipment.

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IV. IMPLEMENTATION

Caltrans is installing and evaluating the Type 140 ramp metering controller in the Los Angeles, San Diego, and San Jose metropolitan areas. The Type 140 Controller and the traffic responsive ramp control program developed in this research has already been shown to be valuable and effective when properly applied for the improvement of freeway operations. Within the next several years, Caltrans plans to install the Type 140 on 1,200 to 1,600 ramps, primarily in the Los Angeles metropolitan area. Initially, these controllers will be operated as independent local controllers. Plans have been made to interconnect many of the controllers in the near future as parts of a 3-level ramp control system.

The Type 140 is also a flexible, general purpose controller. With minor modifications of the original design, the controller can be used as an eight-phase intersection controller or as a diamond interchange controller. A modified design to improve versatility has been incorporated into the most recent order for controllers.

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V. DISCUSSION

A. Microcomputer Technology and Selection.

Microcomputers were made possible by major advances in the state-of-the-art of the large scale integration technology. In general, they are manufactured with either the P-channel, N-channel, or complementary type of metal oxide semiconductor (MOS) materials.

The outstanding features of microcomputers include high packing density, low manufacturing cost, and wide operating temperature range. Since the introduction of the first microcomputer in 1971, their capabilities and applications have advanced at a phenomenal pace. Some of the major applications have been on devices such as pocket calculators, point-of-sale terminals and business machines, various electronic instruments, and controllers for automotive engine parameters. As the newer units become more powerful and their prices continue to decline, it becomes increasingly attractive to replace minicomputers and dedicated logic circuitries with the lower cost microcomputers. Many applications are now becoming practical where in the past the use of computers was considered economically unthinkable.

A typical microcomputer is composed of a microprocessor in one or more chips, read only memory (ROM), random access memory (RAM), an internal clock, and one or more interface chips. The number of ROM and RAM chips in a system is usually expandable to accommodate the specific application. The 4-bit microprocessors can address up to 4096 x 8-bits of program memory, while the newer 8-bit machines can address up to 65536 x 8-bits of memory.

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The internal architectures of a microprocessor generally features the parallel bus structure to simplify data transfers, multi-level register stacks with loadable stack pointer for program branching, and decimal arithmetic capabilities. The earlier P-channel microprocessor introduced by Intel and Rockwell have speeds ranging from 4 to 20 microseconds of minimum instruction time, while the later N-channel models manufactured by Intel, Motorola, and Fairchild have faster minimum instruction time of 2 microseconds.

Instruction sets for the microprocessors generally include the basic functions for data transfers between working registers and with memory devices; logical and arithmetic computations on contents of working registers; increment, decrement, and rotate working registers; conditional and unconditional branches to subroutines; input/output data transfers. Instruction sets of the 8-bit N-channel microprocessors are generally more powerful than their predecessors.

Semiconductor memories used in microcomputers include the read only memory (ROM) and random access memory (RAM). Both of these memory chips are manufactured with the MOS/LSI technology and have the same general physical characteristics as the microprocessor chips. The ROM's are nonvolatile memory devices designed to store non-changing information. Some ROM's are fixed mask programmed and others are field programmable and erasable. In traffic control application where programs are expected to be changing frequently to suit various control locations and changes in traffic patterns, the field programmable read only memory (PROM) is by far more economical and convenient to use. The most widely used PROM chips are manufactured by the

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Intel Corporation using the silicon gate process. These chips come in 256 x 8-bits and 1024 x 8-bit formats. Programming is achieved by applying an electric charge to the specific transistor in the array, and the transistor will remain in this state until a specified dose of ultraviolet radiation is applied through the chip window for a period of 15 to 20 minutes.

The RAM's are volatile memory devices designed for temporary storage of information that changes frequently. In ramp control operations, RAM is used for storage of current occupancies, car counts, preset metering modes and rates, time-of-day, and other calculation results. In the event of a power outage and it is necessary to retain some of the sored data, backup battery power should be provided. Among the various RAM devices available, the complementary MOS device appears to be most suitable because of its low power consumption and high noise immunity features.

Figure 6-1 shows a typical Intel 4-bit microcomputer chip set.

B. Prototype Development

Figure 6-2 shows the prototype microcomputer controller designed and built by the Transportation Laboratory during the early stage of this research for the purpose of gaining better insight of microcomputer hardwares and softwares and to explore the feasibility of ramp control application. This controller includes an Intel 4040 microprocessor, 4096 x 8-bits (16 Intel 1702A chips) of programmable read only memory, 640 x 4-bits (8 Intel 4002 chips) of random access memory, and 128 input/output lines. The Intel 4040 microprocessor is capable of executing 60 different instructions at a cycle time of 10.8 microseconds. The instruction set includes

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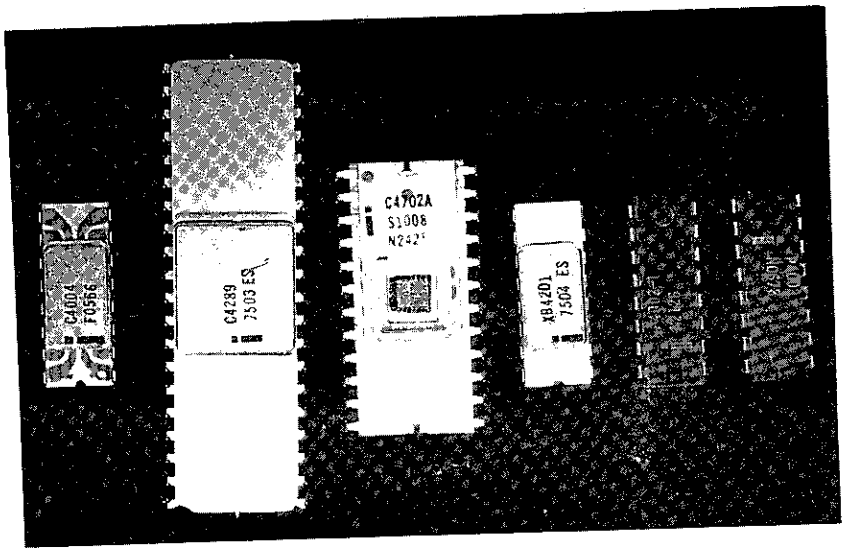

Figure 6-1 Microcomputer Chip Set

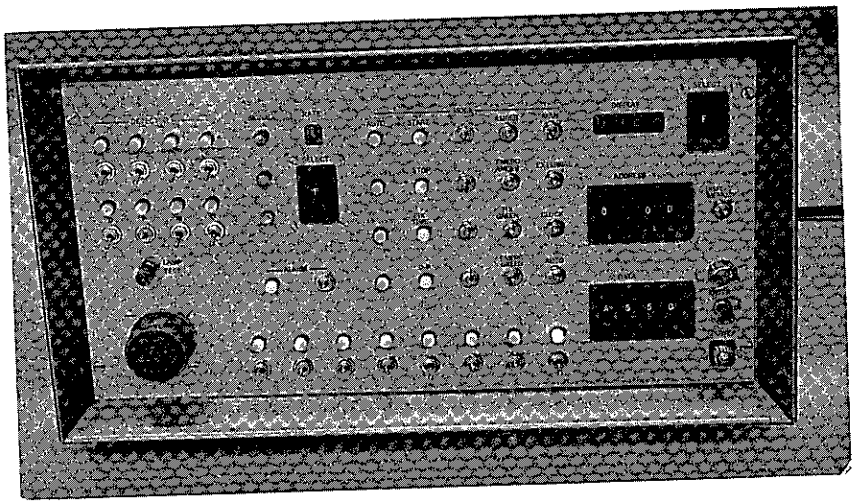

Figure 6-2 Prototype Microcomputer Controller

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conditional branching, arithmetic and logical operations, data transfer between registers and peripheral devices, conditional jump and indirect fetching.

The front panel of the prototype controller was designed to provide the operator with the current traffic status and the means to enter or change the control parameters as deemed necessary. Various ramp control routines have been developed successfully with the prototype controller.

The prototype controller development provided significant insights for the preparation of the design specification for the Type 140 Controller. It enabled the researchers to evaluate the advantages and shortcomings of different microprocessors; especially their instruction capabilities and memory requirements for performing the necessary control functions. It was concluded that the prototype controller using the Intel 4-bit microprocessor is capable of performing the essential ramp control functions for the present but that it might be inadequate for future needs.

The introduction of the N-channel microprocessors revealed many advance features and advantages which the prototype controller lacks. The average cost of the N-channel microprocessors initially was much higher than their predecessor but it is expected with current trends, that the price differential will continue to narrow. Furthermore, the difference in costs of microprocessor chips is insignificant when considering the overall cost of a controller including the cabinet, power supplies, detector amplifiers, modem, etc. There is no doubt that the N-channel microprocessors have sufficient capabilities for present and future needs, and that they will reduce the amount of programming memories and manhours necessary to accomplish the same ramp control algorithm.

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C. Type 140 Controller

The Type 140 Controller was manufactured with the design specification developed from the findings of this research project and from previously established standards. A copy of the design specification is attached to this report as Appendix B. Figure 6-3 shows the Type 140 Controller unit and Figure 6-4 shows the controller unit installed in the cabinets with detector amplifiers, load switches, and control console.

The Type 140 Controller Unit comprised of a Motorola MC6800 8-bit microprocessor, provisions for 4 Intel 2708 programmable read only memory chips (4096 x 8 bit), 1024 x 8 bits of CMOS random access memory, a real-time clock, a down-time accumulator, an integral DC power supply with a backup rechargeable battery, and a communications module. The MC6800 microprocessor is an 8-bit parallel, N-channel MOS processor consisting of an 8-bit bidirectional data bus and a 16-bit directional address bus. With a 16-bit address bus, the microprocessor can address up to 65,536 memory locations and input/output channels. The microprocessor has control features for reset, maskable and non-maskable interrupts, program halt, and direct memory access. Figure 6-5 is a block diagram of the Type 140 Controller Unit.

The communications module, or modem, enables bidirectional data transmissions between the controller and a central computer terminal over a standard voice grade line. The communication module is designed with the frequency shift key (FSK) modulation principle and operates half duplex at a serial data rate of 1200 baud, asynchronous.

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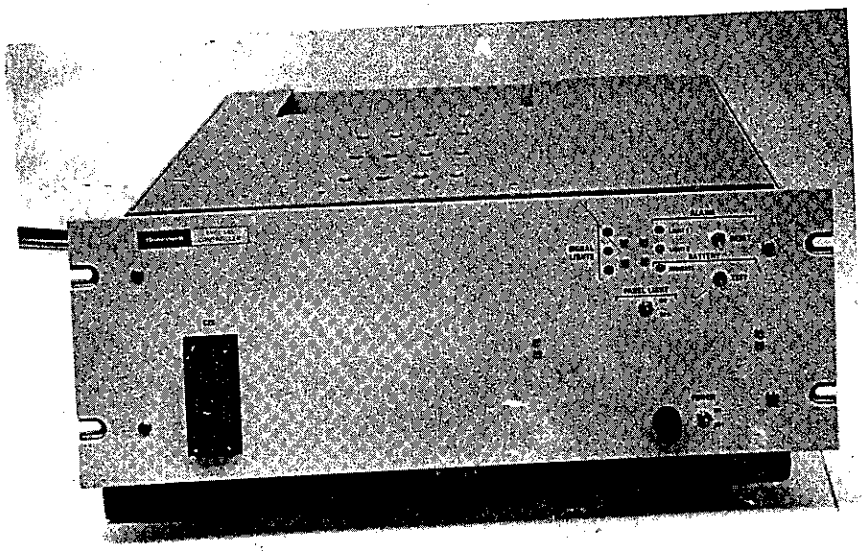

Figure 6-3 Type 140 Controller

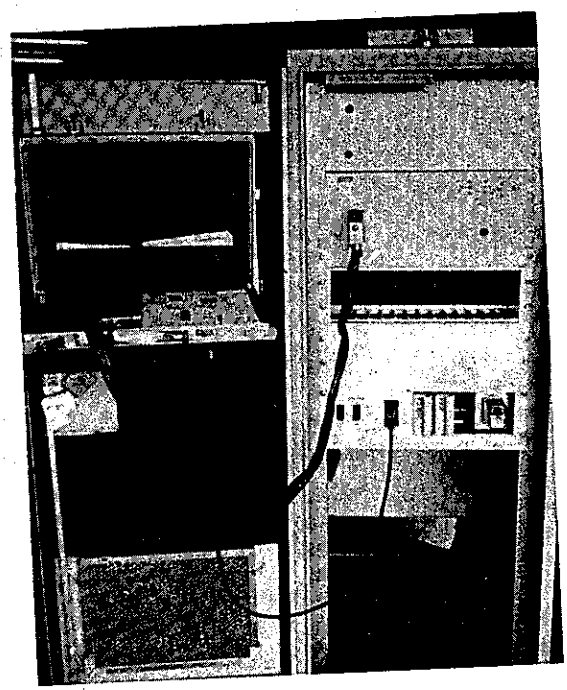

Figure 6-4 Type 140 Controller Cabinet and Control Console

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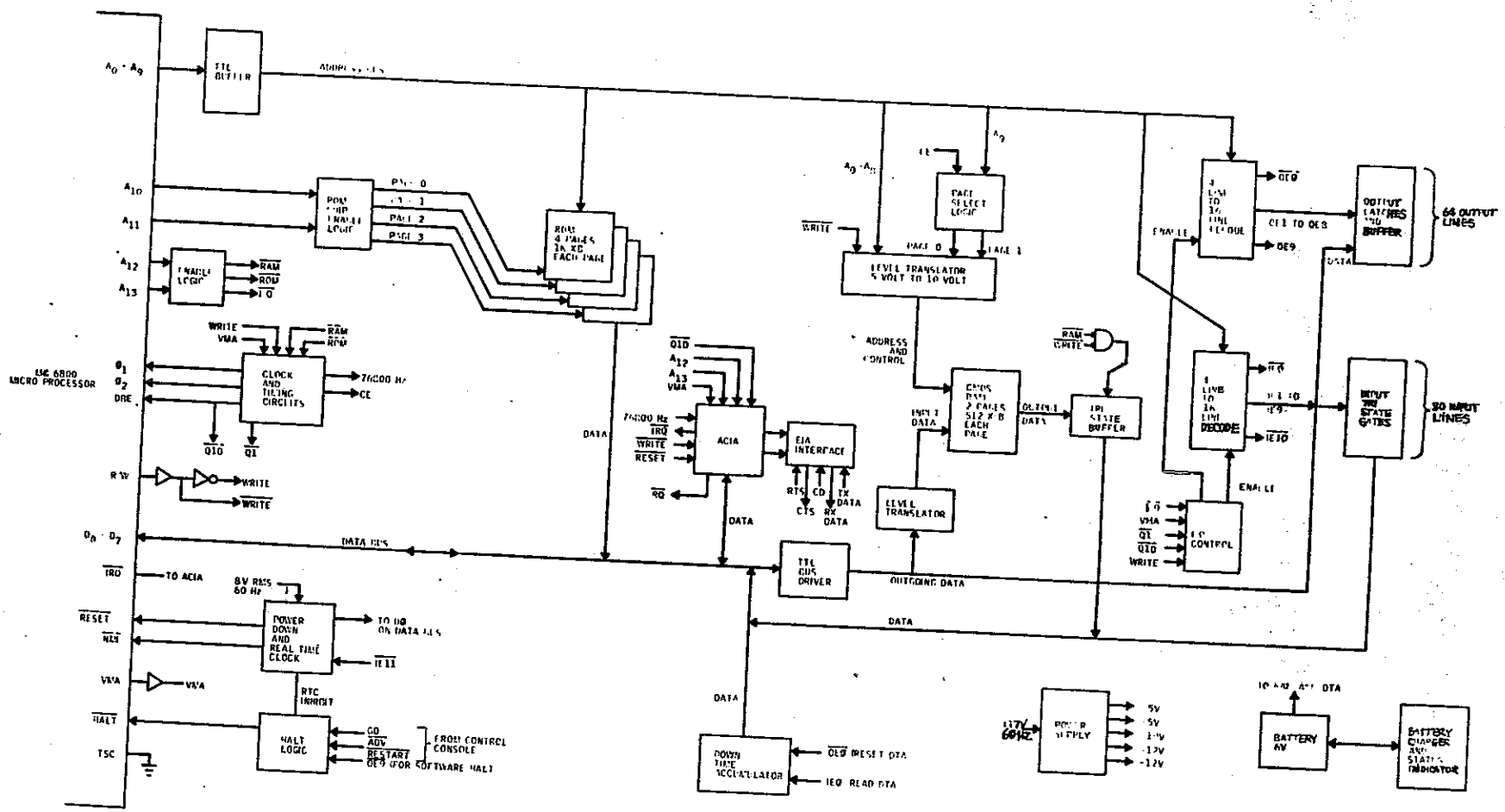

Figure 6-5 140 Controller Block Diagram

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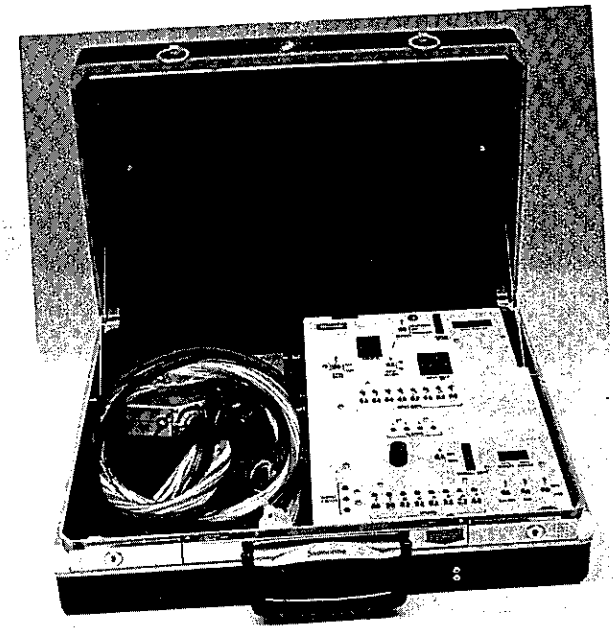

Figure 6-6 Portable Control Console

Figure 6-7 PROM Programmer and Erasing Light

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The control console for the Type 140 Controller is mounted within a briefcase approximately 18" (45.7 cm) x 18" (45.7 cm) x 4.5" (11.4 cm). It was designed to interface with the controller via a 104-pin connector cable as shown in Figures 6-4 and 6-6. The portable concept was designed to reduce the cost of the controllers by eliminating the need for having the console parameters built into each controller front panel.

The control console was designed for the operator to evaluate the current traffic condition and enter changes of the control parameters as deemed necessary.

Following are brief descriptions of the control console parameter functions:

1. Data Display -- This LED readout displays the content of the memory location set on the Address thumbwheel switches. All the current traffic parameters such as occupancies, vehicle counts, detector status, minimum green and red times, meter rate table, etc., can be displayed with the proper address setting.

2. Address Thumbwheel -- The hexidecimal settings on these thumbwheel switches indicate the address of the memory location to be displayed or entered with new data. Since there are 1024 RAM locations in the controller, the use of RAM maps such as those shown on page _ and _ should be helpful.

3. Input Data -- The metering parameters stored in RAM are changeable via either the 8 toggle or 2 thumbwheel switches. The value set on these switches are entered into the specified RAM location by activation of the Load Data toggle switch.

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4. Signal Lights -- These 3 lights indicate the current status of the metering signal in red, amber, or green.

5. Mode Selection and Display -- These provisions set the controllEr in either the Automatic or Manual metering mode. When this switch is set at the Automatic mode, the metering rate is based on either the date and time-of-day, or current occupancy. When the Manual mode is set, the setting on the Manual Rate switch is used.

6. Manual Rate -- This hexidecimal thumbwheel switch has 16 different metering rate positions (Rate 0 to Rate F). The cycle time assigned to each rate is preset in RAM and is manually changeable to suit the specific traffic condition. The rate set on this switch is used only for the manual mode of operation.

D. Ramp Control Program

The ramp control program for the Type 140 Controller is designed to meter a given ramp at a rate based on the Julian calender and time-of-day, or based on the current average mainlane occupancy. This program occupies 1620 x 8-bits of programmable read only memory (PROM) and employs approximately 512 x 8-bits of random access memory (RAM) for storage of the rate table, holidays, and traffic data and control parameters.

The ramp control program is divided into 12 routines stored in the following memory (PROM) locations:

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Routines	Memory Locations
Power On/Reset and Initialize	39F8 - 3A3B
Executive	3A3C - 3A6F
Detector Service	3A70 - 3ABA
Vehicle Count	3ABB - 3B39
Detector Check	3B3A - 3BA1
3 Minute Occupancy Computation	3BA2 - 3BF0
Meter Rate Selection	3BF1 - 3CAE
Signal Service	3CD3 - 3D9B
Signal and Sign Output	3CAF - 3CDA
Console Service	3D9C - 3E60
Time Service	3800 - 38D8
Occupancy Computation and Detector Checking	38E0 - 39F7

	Memory Location	Content
Internal Interrupt Pointer	3FF8	39
	3FF9	F8
Software Interrupt Pointer	3FFA	39
	3FFB	F8
Non-Maskable Interrupt Pointer	3FFC	38
	3FFD	00
Reset Pointer	3FFE	39
	3FFF	F8

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The functions of the above routines are described in detail in the following paragraphs and attached flowcharts and program listings.

1. Power On/Reset and Initialized

This routine is the initial starting point of the program whenever the microprocessor power switches to on. This routine sets the stack pointer, check the down time accumulator and updates the time-of-day clock whenever the downtime was shorter than 256 minutes, set the working counters in RAM to their initial values, and set the signal initially to green.

2. Executive

Upon completion of the Power On/Reset and Initialize routine from initial startup, the Executive proceeds to sequentially service all the routines within the program with exception of the Time Service and Occupancy Computation and Detector Checking routines which are serviced by the non-maskable interrupt. The Executive services the Detector Service routine once every 50 milliseconds, the Signal Service routine once every 100 milliseconds and the other routines during the remaining time period.

3. Detector Service

This routines scans the mainlanes and ramp detectors once every 50 milliseconds for presence of vehicles. Verification of the detector inputs is made and the unused input(s) is discarded to prevent false detector alarm. If presence is detected on a given input, the respective 10 second occupancy counter is

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incremented by one. The demand and passage flag is set if presences are detected by their respective inputs.

4. Vehicle Count

This routine verifies and counts the total number of vehicles which passed over each detector over the past one-minute period. Verification is made by counting the number of consecutive presences and gaps on each detector input. Two consecutive presence counts constitute a vehicle. Each vehicle count must be reset by five or more consecutive gap counts. The vehicle count for the ramp, individual mainlane, and the total of all mainlanes are computed and updated for each one-minute period. The vehicle counts are stored in RAM locations 0090-00BF. RAM locations 0020-0049 are used as working counters for presence and gap.

5. Detector Check

Each detector is continually checked for its functional integrity. In this routine, the vehicle count associated with each mainlane detector is checked for a reasonable number. During the period from 6 A.M. to 12 midnight, excluding Sunday, the one-minute vehicle count should not be less than 2. Five consecutive one-minute periods with vehicle counts less than 2 will activate the detector alarm. The ramp detectors are checked by comparing the demand and passage detector counts for the one-minute period. If the discrepancy is greater than 2, an alarm will be activated for the detector with the fewer number. This checking method is not applicable when more than one demand detector is used.

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6. 3 Minute Occupancy Computation

This routine computes the mainlane occupancy for the past 3-minute period. Whenever the controller is operating in the traffic responsive mode, the 3-minute occupancy is used to determine the threshhold for start or stop metering. The 3-minute period is chosen for the purpose of damping excessive start/stop meter cycling that could be caused by frequent traffic fluctuations.

7. Meter Rate Selection

This routine checks the Julian calender for holiday. If the Julian date compares with one of the 16 holiday entries stored in RAM locations 0060 - 007F, metering will be suspended. If it is not a holiday, the program will check for a manual control signal from the control console. If a manual signal is detected, the manual rate setting on the console is selected. There are 16 metering rates numbered 0-F stored in RAM locations 0120 - 012F settable by the operator with the appropriate cycle times. For example, Rate 0 may be set for 4 seconds cycle time and progressively increase to 26 seconds cycle time for Rate F. The unit of entry for cycle time is in 1/10 second, hexidecimal.

If the manual signal is not present, the metering rate is selected by matching the weekday and time-of-day with the appropriate entry on the table stored in RAM locations 0180-01FF. The meter time table contains 32 entries and each entry contains the following information for identifications:

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a. Hour, minute, and weekdays on which the command is to be executed.

b. Specify the command to be executed. This entry can be a stop metering command, a given meter rate, or a traffic responsive selection command. If the command entry contains the letter "F" as prefix, the hexidecimal number that follows is the metering rate to be executed. The letter "E" prefix indicates a new meter rate entry, and a "D" prefix indicates a stop meter command. If the command contains none of the above prefixes, rate selections will be traffic responsive. There are 16 occupancy entries located on RAM locations 0110-011F. Each individual entry is associated with a metering rate located immediately to their right on the RAM map. As a example, a reasonable occupancy entry for a Rate 0 of 4 second cycle time would be 0A in hexidecimal (10% decimal) and for a Rate F of 1A (26 decimal) seconds would be 16 in hexidecimal (22% decimal).

8. Signal Service

The following functional features are provided in this routine:

a. The signal rests in green whenever it is not metering.

b. A first amber signal is provided prior to the first metering cycle as a warning to approaching motorists that metering has started. An optional amber may be set on all subsequent cycles at the operator's discretion. The first amber time is set in RAM location 0133, and it should be computed with the consideration of the approach speeds on the ramp.

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The red time of a given cycle varies with the total cycle length, but not shorter than the minimum setting. The signal will remain in red if no demand is present.

The green time of a given cycle features the minimum green, fixed green, or maximum green. This signal will not be shorter than the minimum green nor longer than the maximum green under any circumstances. The fixed green time is used when the passage detector has failed or is not used.

9. Signal and Sign Outputs

This routine services the following:

a. Activates the signals in accordance with the setting on RAM location 014F.

b. Activates the alarm lights on the controller front panel in accordance with the detector alarm status.

c. Outputs a 0.1 second signal to the watchdog timer.

d. Activates the meter-on sign located at the ramp entrance in accordance with the metering status.

10. Console Service

This routine scans the Display Select switch on the control console and outputs the selected information to the Data Display readout in accordance with the following assignment.

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Display Select Setting	Data Display
0 - 3	Memory content
4	Time-of-day
5	Julian date

To display or input the memory content, the Display Select setting is taken as the most significant digit of the memory address and the remaining 3 digits are taken from the Address Switches.

The Load Data Switch is scanned for data input command. If this momentary switch is set, the content of the Input Data Switches is transferred to the RAM location as specified on the above paragraph.

11. Time Service

This routine is serviced by the non-maskable interrupt 60 times per second. Whenever the interrupt signal is received, the microprocessor will depart from its normal program flow to service this routine in its entirety. The normal program will resume from the departed location when the time service routine is completed.

Using 60 hertz as the time base, this routine updates the time-of-day in seconds, minutes, and hours; the dayof-week; and the Julian calender. The time parameters store in RAM locations 0155-015E have been converted from hexidecimal to decimal. Time flags are provided on RAM location 0154 for 50 millisecond, 100 millisecond, 1 minute, 5 minutes, 15 minutes,

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1 hour, and 1 day. These flags are represented by their respective bits within the RAM location in the same order listed above. The least significant bit represents the 50 millisecond flag, and the 7th bit represents the day flag. The days-of-week stored in RAM location 015F are also associated by bit numbers starting with the least significant bit representing Sunday.

This routine branches to the Occupancy Computation and Detector Checking subroutine once every 10 seconds.

12. Occupancy Computation and Detector Checking

This routines computes and updates the one minute occupancy counts for each mainlane and total of all mainlanes once every 10 seconds. RAM locations 00C0-00FF are being used as working counters for the occupancy computations. The average occupancies in percents are computed based upon the detector scanning rate of 20 times per second and a 100% occupancy factor of 1200 counts per minute for a given lane.

This routine also checks for detector malfunction by comparing the individual mainlane occupancies with the mainlane total. A detector is considered bad if the computed percent occupancy for that lane is either greater by the factor of 2 or less by the factor of 1/2 than the same value computed for the overall mainlanes.

Whenever a bad detector is detected on the mainlanes, the percent occupancy for that lane is replaced by the value for the adjacent lane.

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	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0	Down Tire		Lane-1 Pres.	Spare Lane	Spare Lane	Ramp Detr. Used	HOLIDAYS LSB	LSB	First Minute Occup.	Veh. Counter Lane-1	Spare Lane	N/U	Lane-1 10 Sec Occup.		N/U		0
1			Lane-1 Gap		Demand Pres.	Main-L Detr. Used	MSB	MSB	" MSB	Minute Total	N/U	Veh. Counter Demand			Lane-4 10 Sec Occup.		1
2	Lane Counter		Gap Flag		Demand Gap	Ramp Detr. Status			Second Minute Occup.	Check Counter	Spare Lane	Minute Total		Minute Total			2
3	ML/R Counter		Lane-2 Pres.		Gap Flag	Main-L Detr. Status			" MSB	Veh. Counter Lane-2	Spare Lane	Check Counter		" MSB		Minute Total	3
4			Lane-2 Gap		Passage Pres.	Ramp Detr. Alarm			Third Minute Occup.	Minute Total	N/U	Veh. Counter Passage		Ave. Occup. %		" MSB	4
5			Gap Flag		Passage Gap	Main-L Detr. Alarm			" MSB	Check Counter	Spare Lane	Minute Total		N/U		Ave. Occup. %	5
6			Lane-3 Pres.		Gap Flag				3 Minute Occup.	Vehicle Counter Lane-3	Spare Lane	Check Counter		Lane-3 10 Sec Occup.		N/U	6
7			Lane-3 Gap		Off-R Pres.				" MSB	Minute Total	N/U	Veh. Counter Off-R	Minute Total			Main Lane Total	7
8			Gap Flag		Off-R Gap				Ave. Occup. %	Check Counter	Spare Lane	Minute Total	" MSB		Minute Total	" MSB	8
9			Lane-4 Pres.		Gap Flag				Threshd. Occup.	Veh. Counter Lane-4	Spare Lane	Check Counter	Ave. Occup. %		" MSB	Ave. Occup. %	9
A			Lane-4 Gap							Minute Total	N/U		N/U		Ave. Occup. %	N/U	A
B			Gap Flag							Check Counter	Spare Lane		Lane-2 10 Sec Occup.		N/U	Counter Pointer	B
C			Lane-5 Pres.						Minute Flag	Veh. Counter Lane-5	Spare Lane				Lane-5 10 Sec Occup.	" LSB	C
D			Lane-5 Gap						Counter Address	Minute Total	N/U			Minute Total		Sum Pointer	D
E	Rate Address		Gap Flag				HOLIDAYS LSB	LSB	Counter Address	Check Counter	Spare Lane			" MSB		" LSB	E
F	Rate Address		Spare Lane	Spare Lane			MSB	MSB	Minute Pointer	Spare Lane	Spare Lane	Total Main-L Veh.		Ave. Occup. %		10 Sec Counter	F

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RAM 0100-01FF

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0		% Occup.	Rate 0	Meter On Flag	Max. Green Timer		Stack	Stack	Hour 05	Hour 06	Hour 07	Hour 08	Hour 15	Hour 16	Hour 17	Hour 18
1		% Occup.	Rate 1	Start Meter Flag	Min. Green Time		Stack	Stack	Minute 00	Minute 00	Minute 00	Minute 00	Minute 00	Minute 00	Minute 00	Minute 00
2		% Occup.	Rate 2	No Meter Flag	Min. Green Timer		Stack	Stack	Week Days	Week Days	Week Days	Week Days	Week Days	Week Days	Week Days	Week Days
3		% Occup.	Rate 3	First Amber Time	Demand Flag		Stack	Stack	Rate F0	Rate F4	Rate F8	Rate F6	Rate 0	Rate F4	Rate F8	Rate F6
4		% Occup.	Rate 4	Amber Timer	Passage Flag	Time Flag	Stack	Stack	Hour 05	Hour 06	Hour 07	Hour 08	Hour 15	Hour 16	Hour 17	Hour 18
5		% Occup.	Rate 5	Min. Red Time		60 Hertz	Stack	Stack	Minute 15	Minute 15	Minute 15	Minute 15	Minute 15	Minute 15	Minute 15	Minute 15
6		% Occup.	Rate 6	Min. Red Timer		100 M.S.	Stack	Stack	Week Days	Week Days	Week Days	Week Days	Week Days	Week Days	Week Days	Week Days
7		% Occup.	Rate 7	Cycle Timer	Amber Option Flag	1 Second	Stack	Stack	Rate F1	Rate F5	Rate F8	Rate F4	Rate 1	Rate F5	Rate F8	Rate F4
8		% Occup.	Rate 8	Cycle Time	Amber Time	Minute (5)	Stack	Stack	Hour 05	Hour 06	Hour 07	Hour 08	Hour 15	Hour 16	Hour 17	Hour 18
9		% Occup.	Rate 9	Min. On Time		Minute (15)	Stack	Stack	Minute 30	Minute 30	Minute 30	Minute 30	Minute 30	Minute 30	Minute 30	Minute 30
A		% Occup.	Rate A	Min. On Timer		Minute (60)	Stack	Stack	Week Days	Week Days	Week Days	Week Days	Week Days	Week Days	Week Days	Week Days
B		% Occup.	Rate B	Min. Off Time	Flash Code	Hour	Stack	Stack	Rate F2	Rate F6	Rate F8	Rate F2	Rate F2	Rate F6	Rate F8	Rate F2
C		% Occup.	Rate C	Min. Off Timer		Day	Stack	Stack	Hour 05	Hour 06	Hour 07	Hour 08	Hour 15	Hour 16	Hour 17	Hour 18
D		% Occup.	Rate D	Cycle Ready Flag		Day-of Year	Stack	Stack	Minute 45	Minute 45	Minute 45	Minute 45	Minute 45	Minute 45	Minute 45	Minute 45
E		% Occup.	Rate E	Stop Meter Flag	Alarm Lights	Day-of Year	Stack	Stack	Week Days	Week Days	Week Days	Week Days	Week Days	Week Days	Week Days	Week Days
F		% Occup.	Rate F	Max. Green Time	Signal Lights	Day-of Week	Stack	Stack	Rate F3	Rate F7	Rate F7	Rate 00	Rate F3	Rate F7	Rate F8	Rate 00

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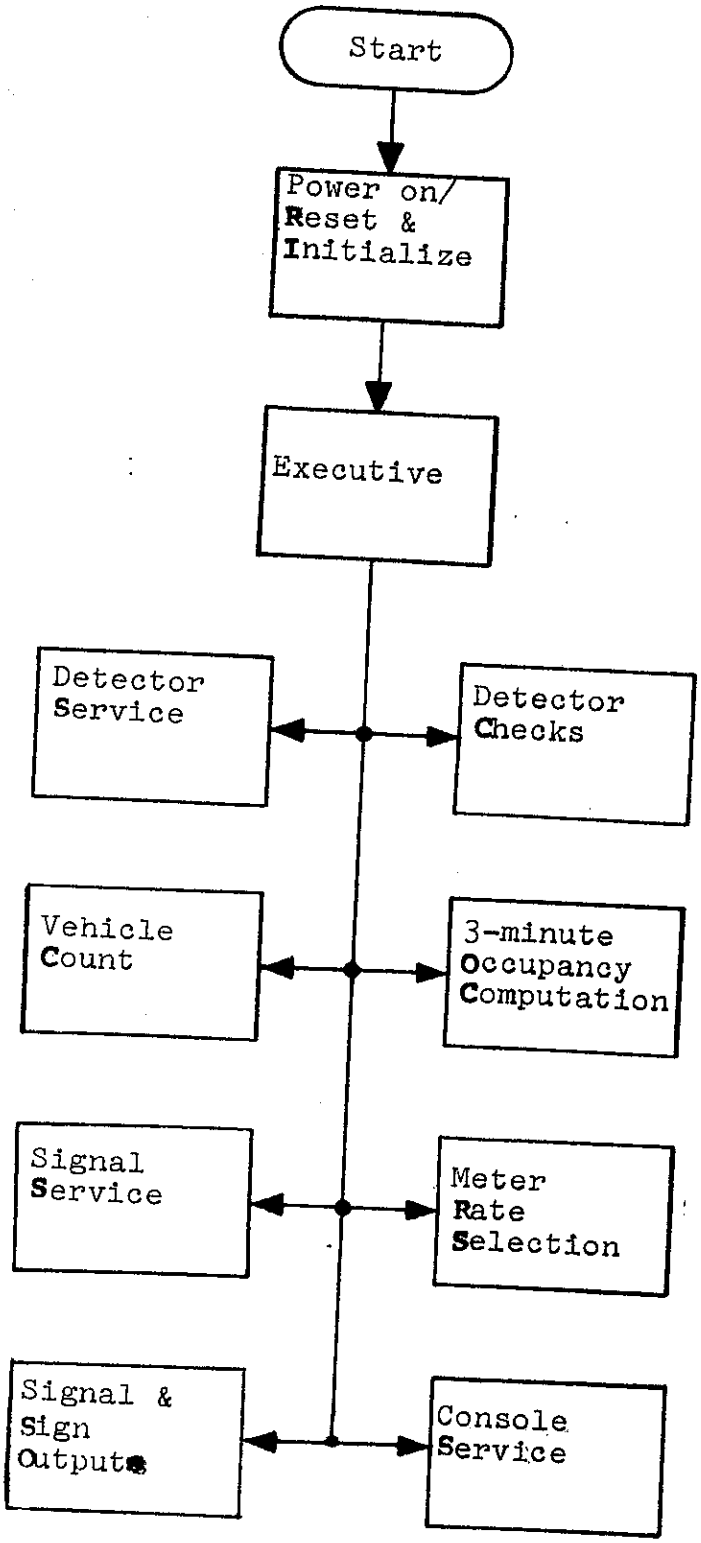

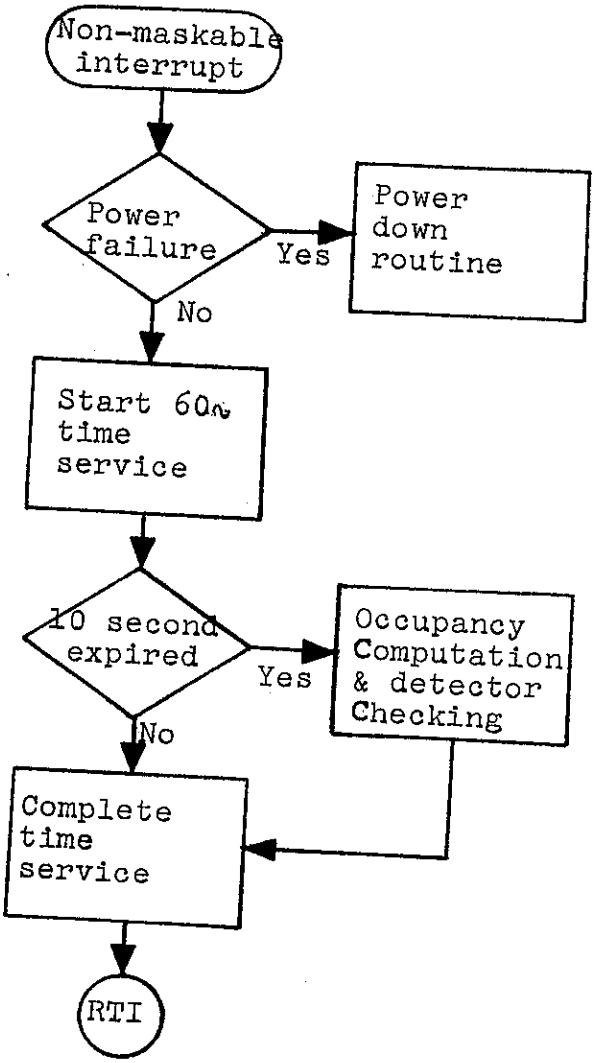

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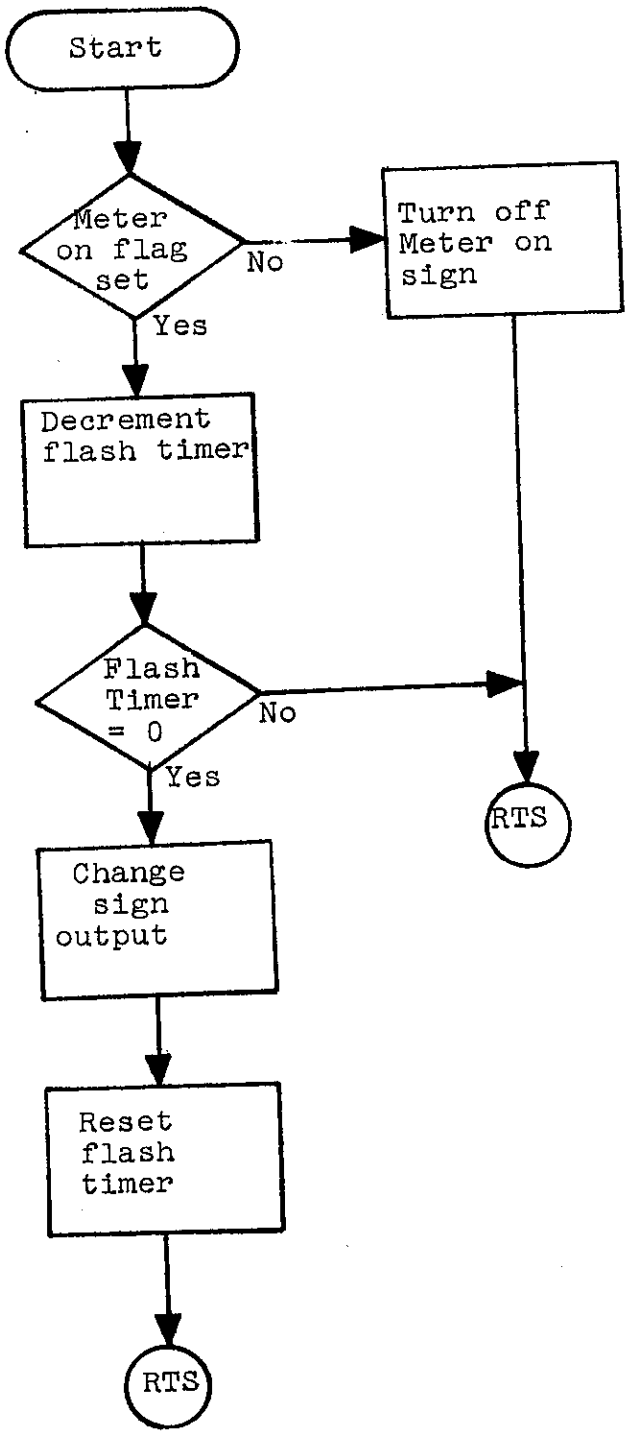

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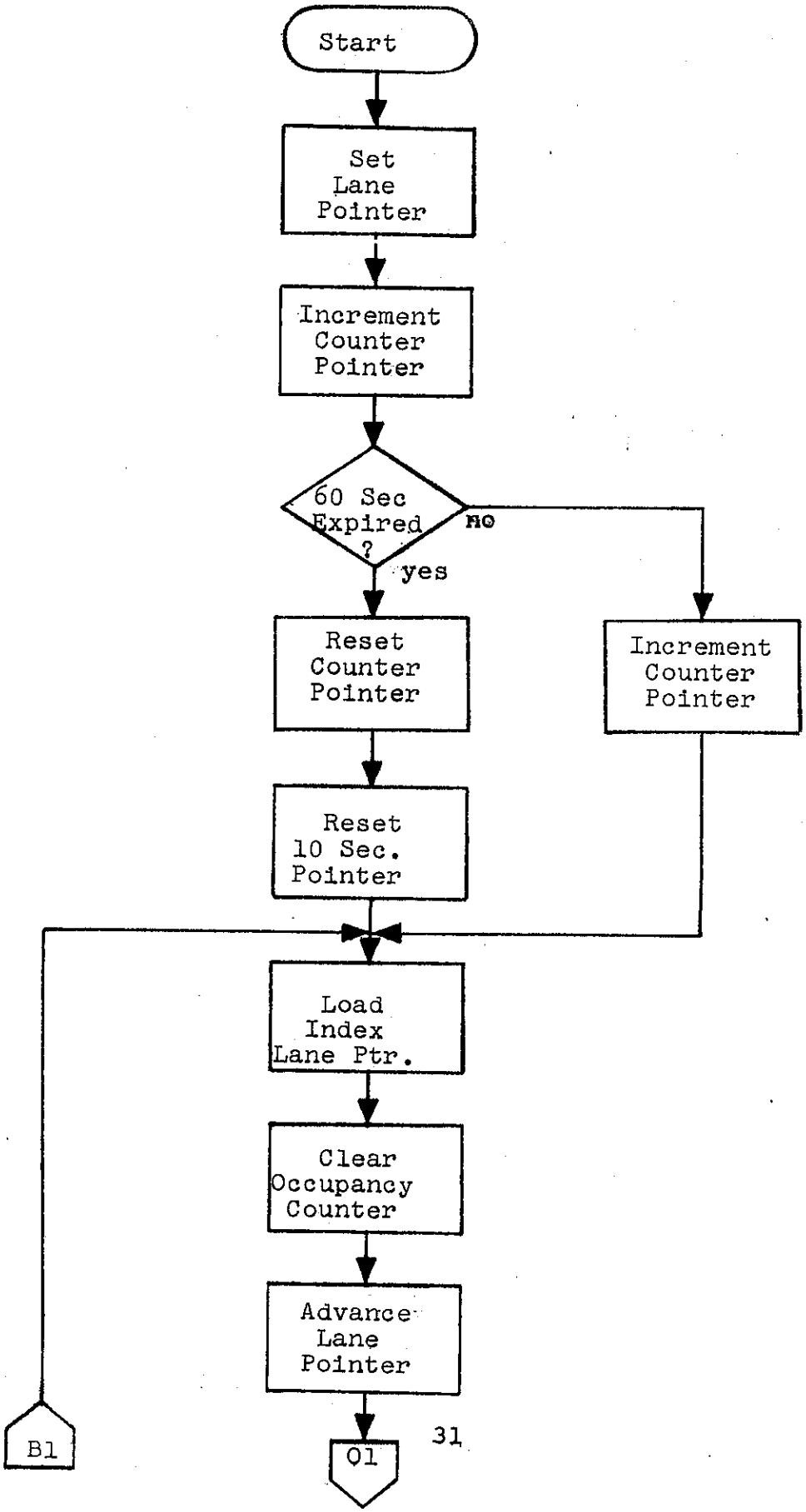
OCCUPANCY COMPUTATION & DETECTOR CHECKS



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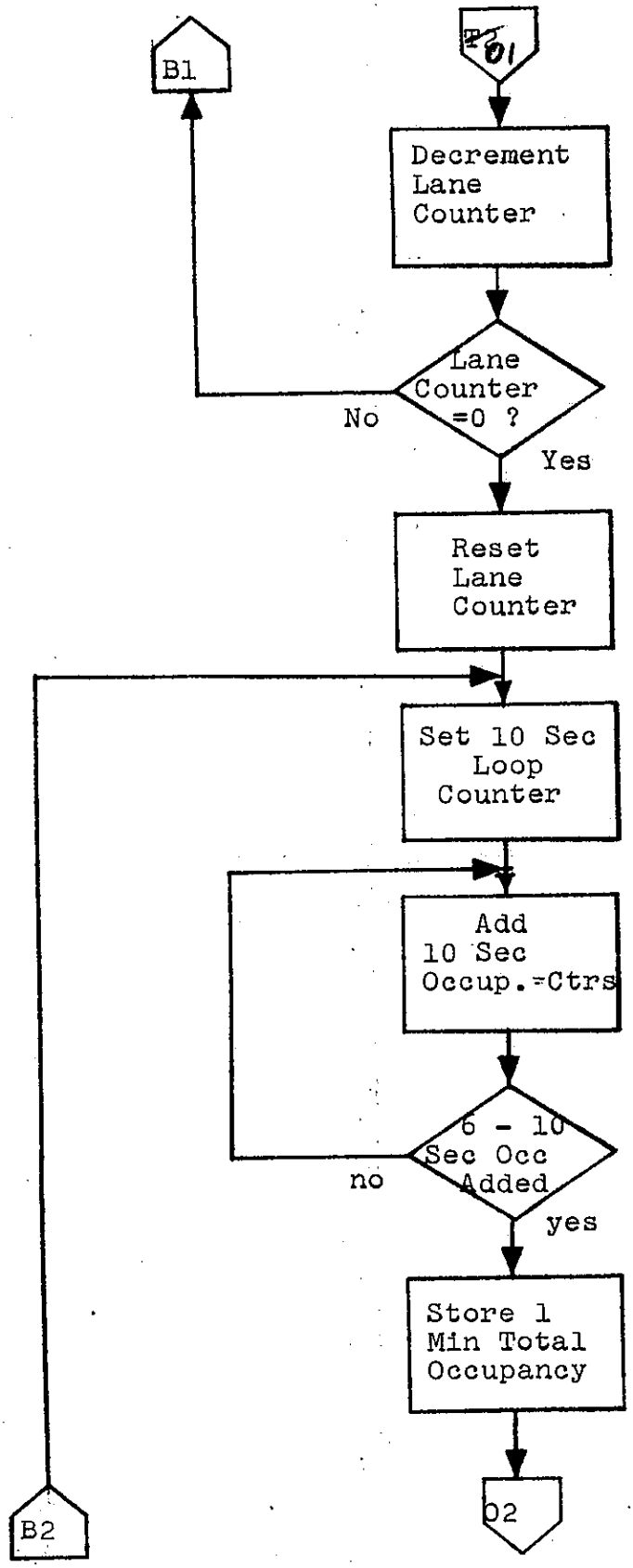

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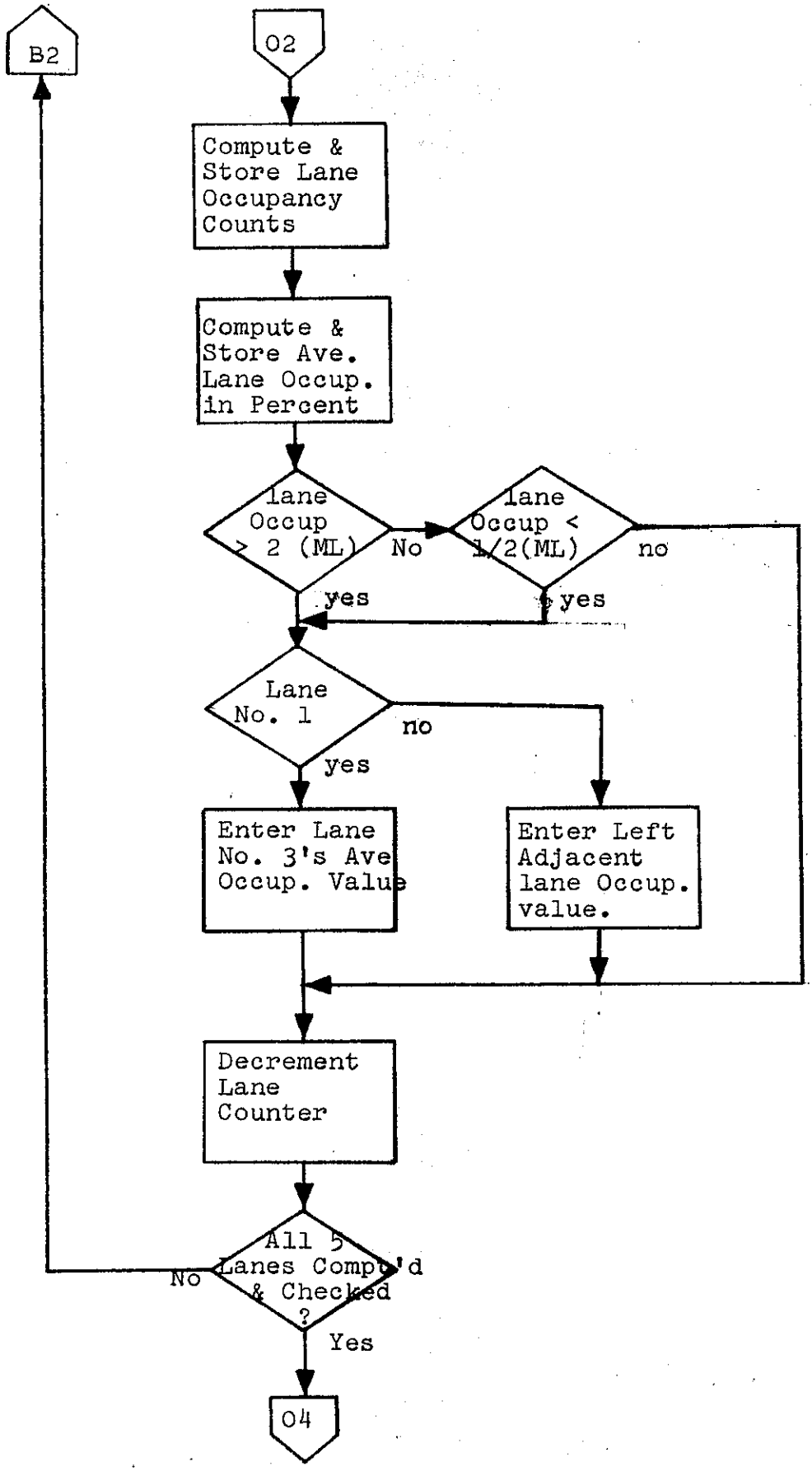
OCCUPANCY COMPUTATION & DETECTOR CHECKS



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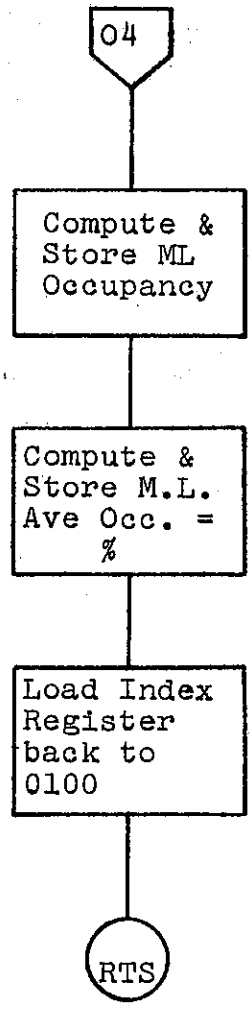

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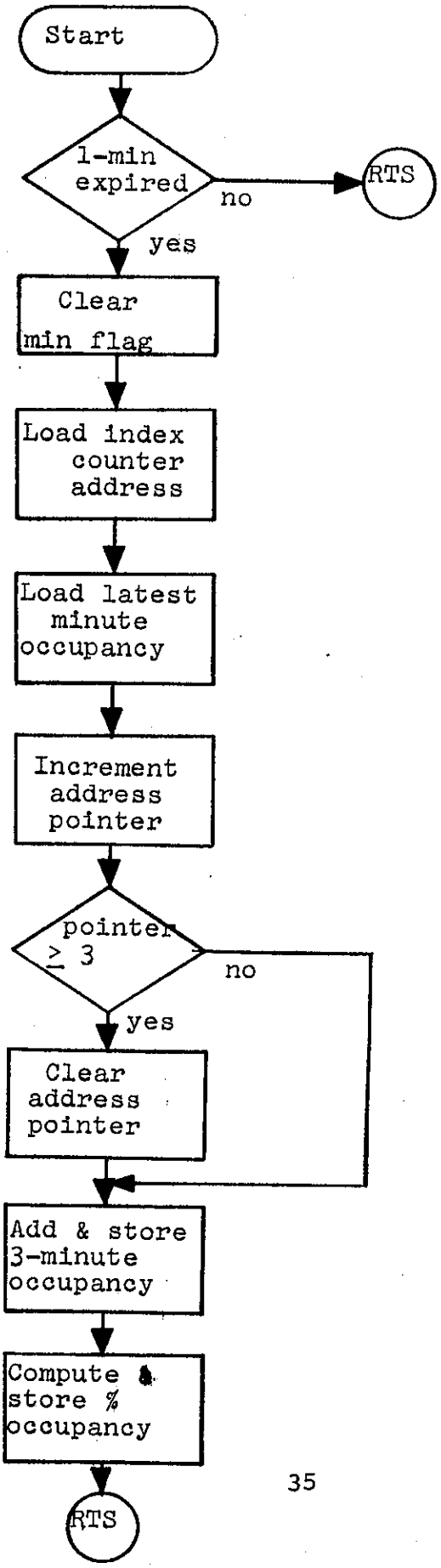
3-MINUTE OCCUPANCY COMPUTATION



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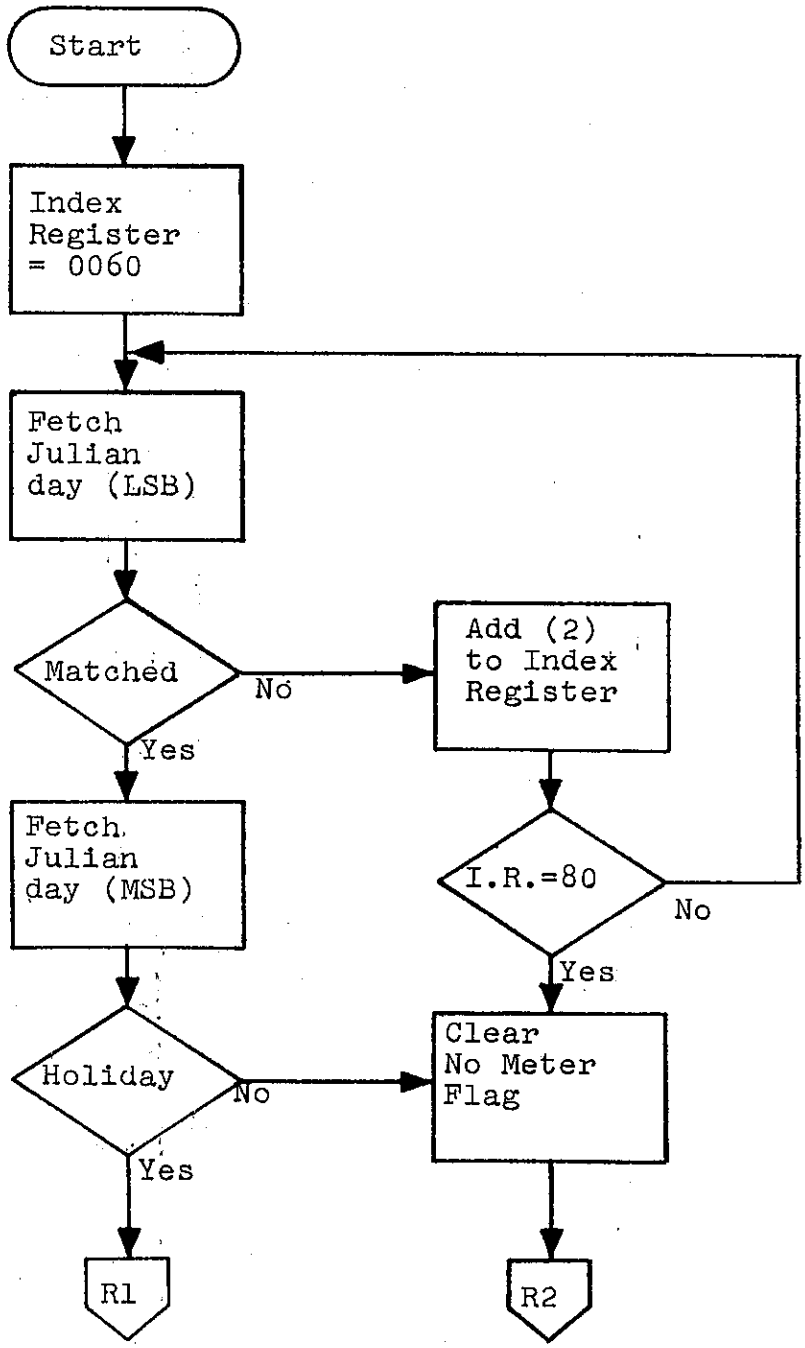
Meter Rate Selection



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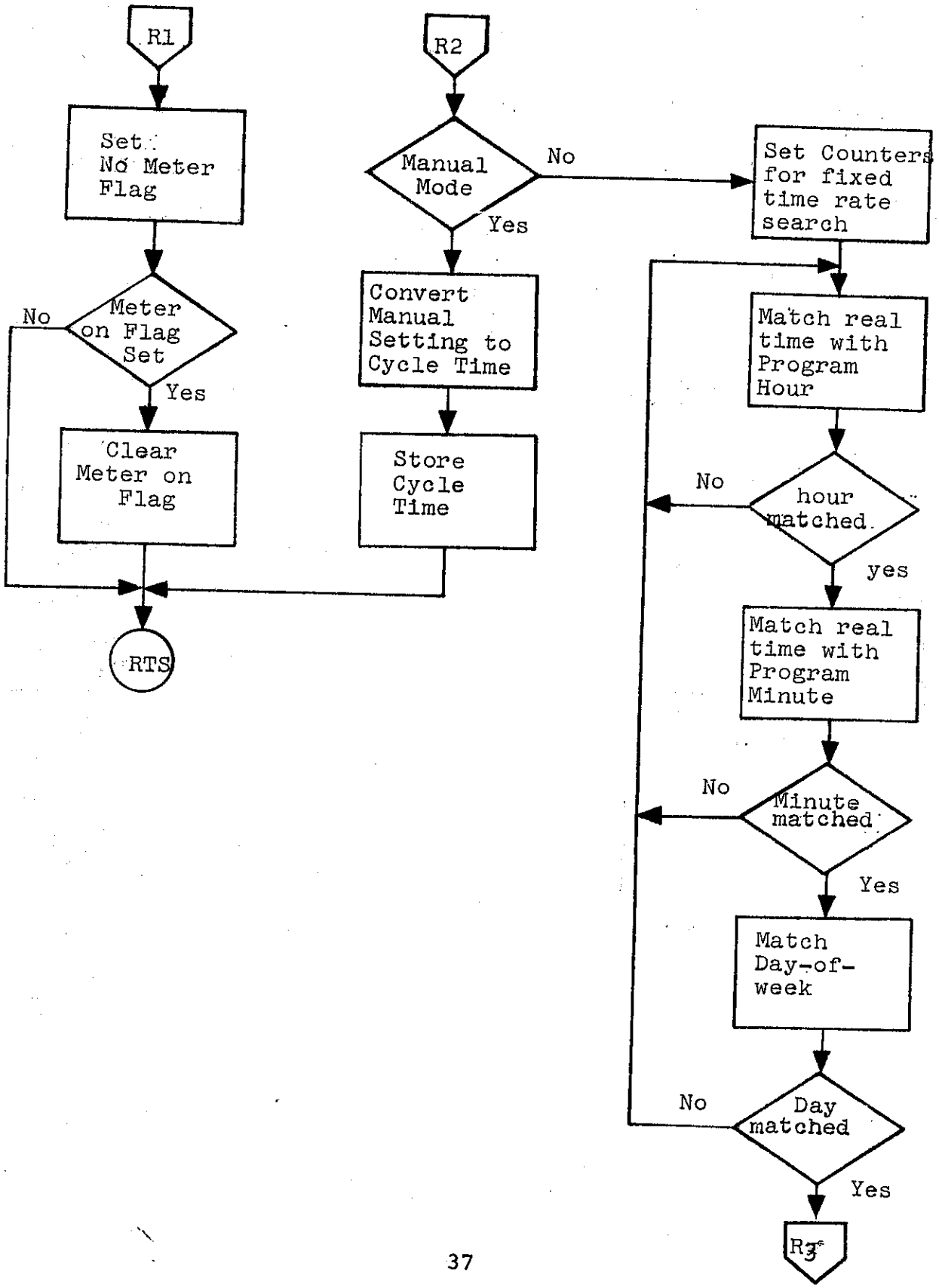
METER RATE SELECTION



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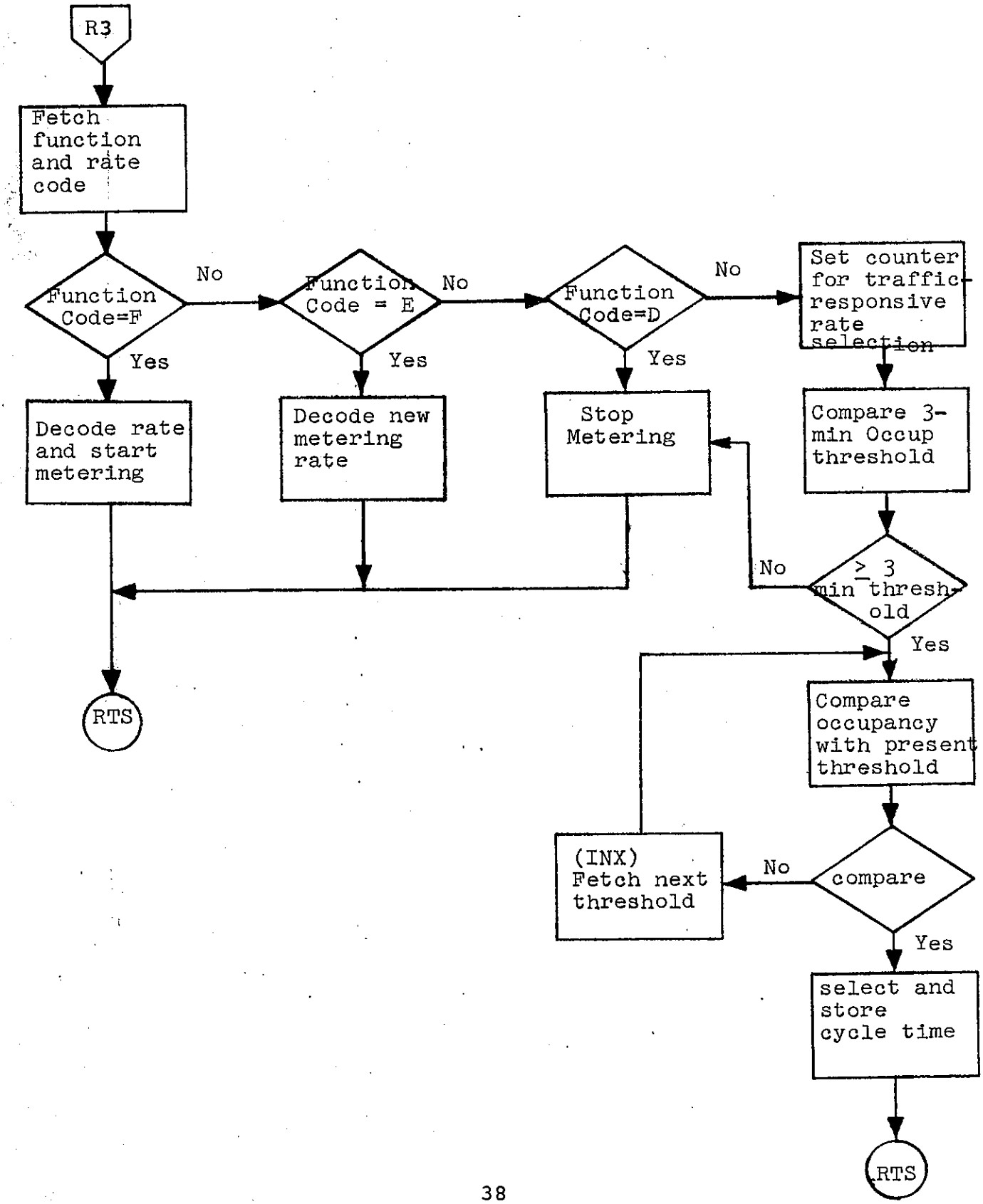

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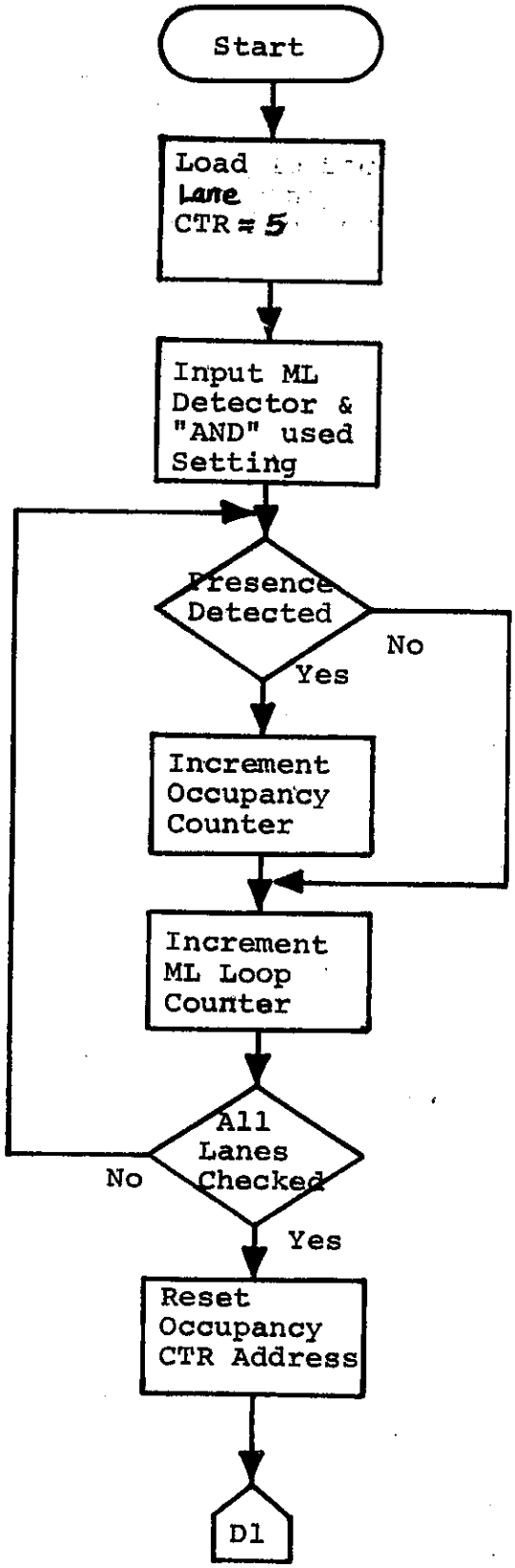

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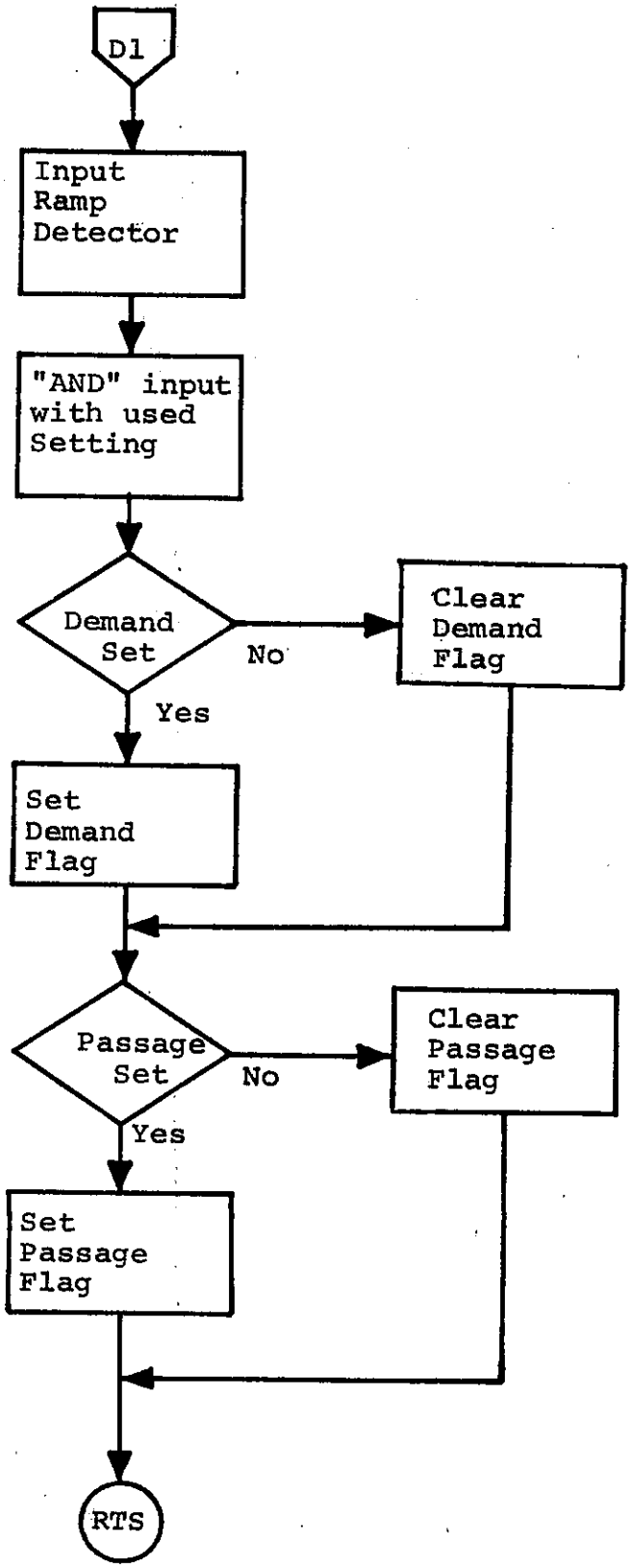

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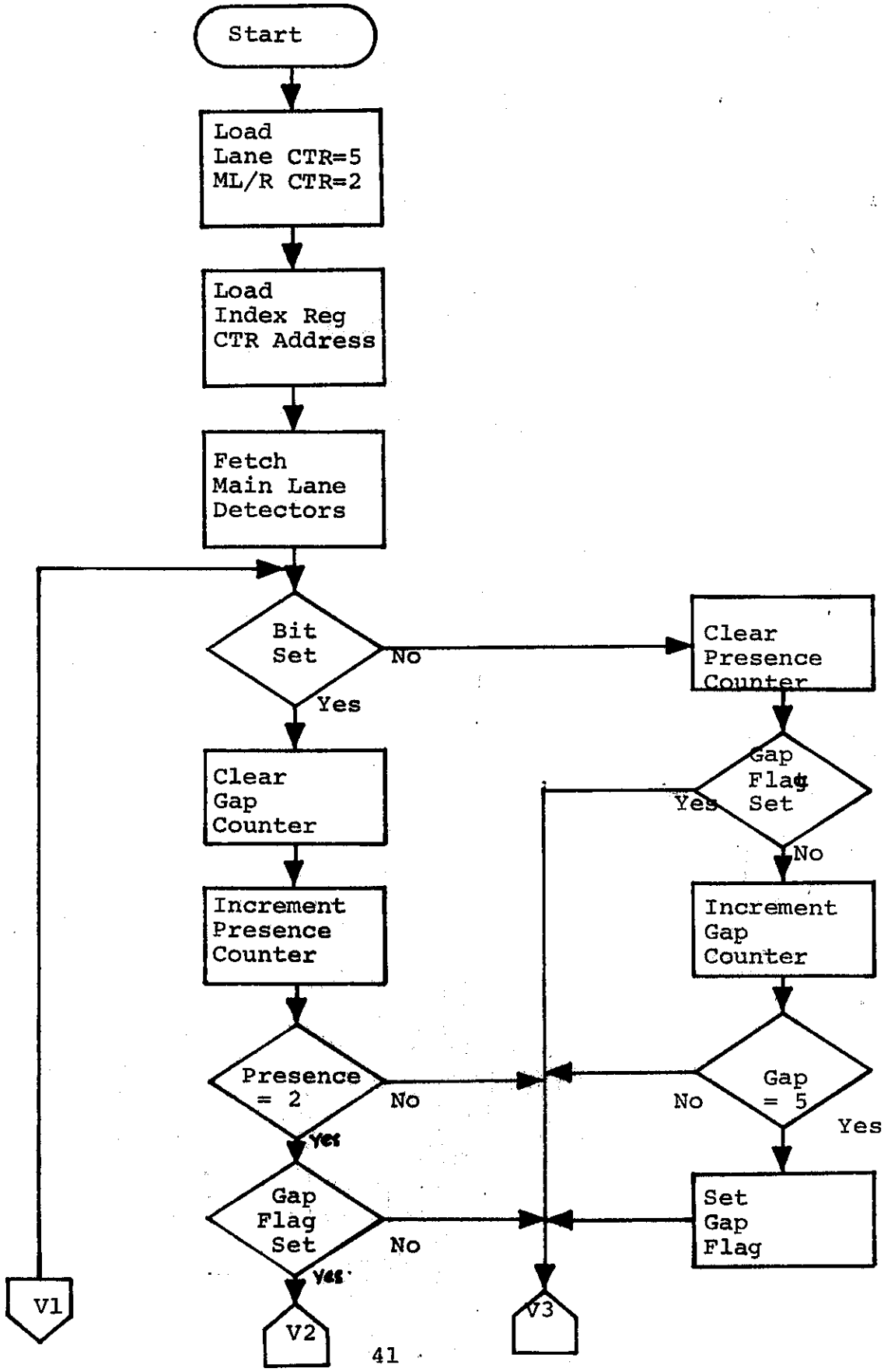
Vehicle Count



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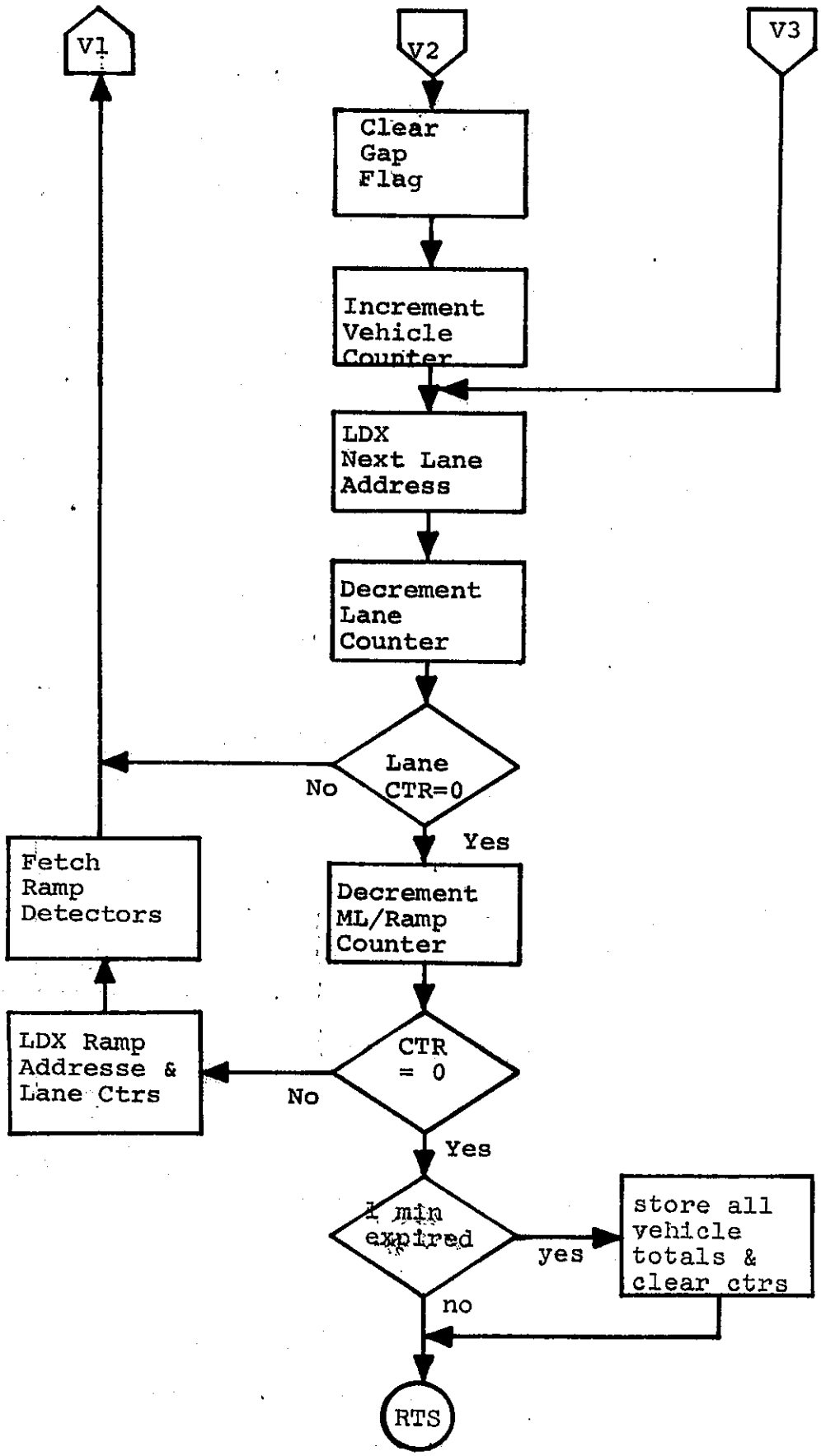

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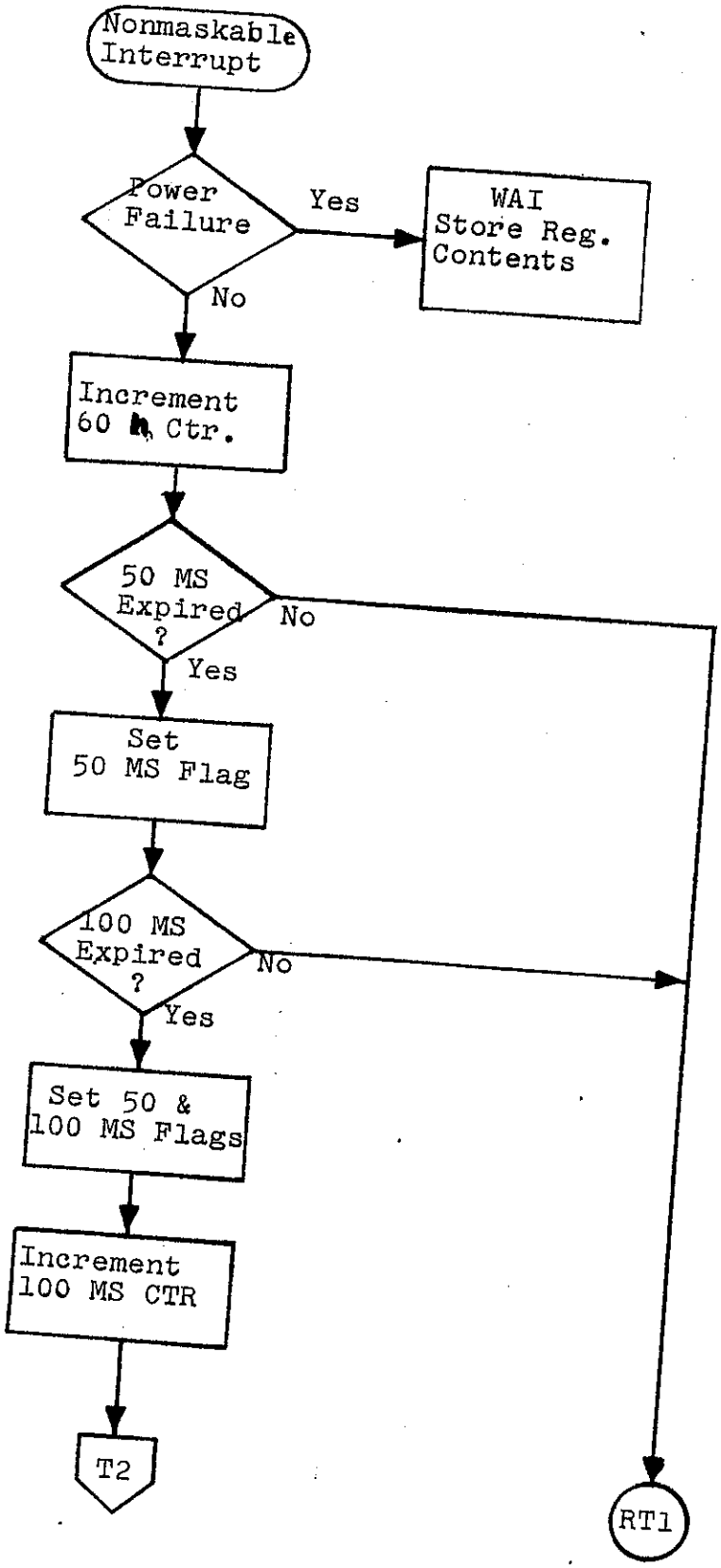

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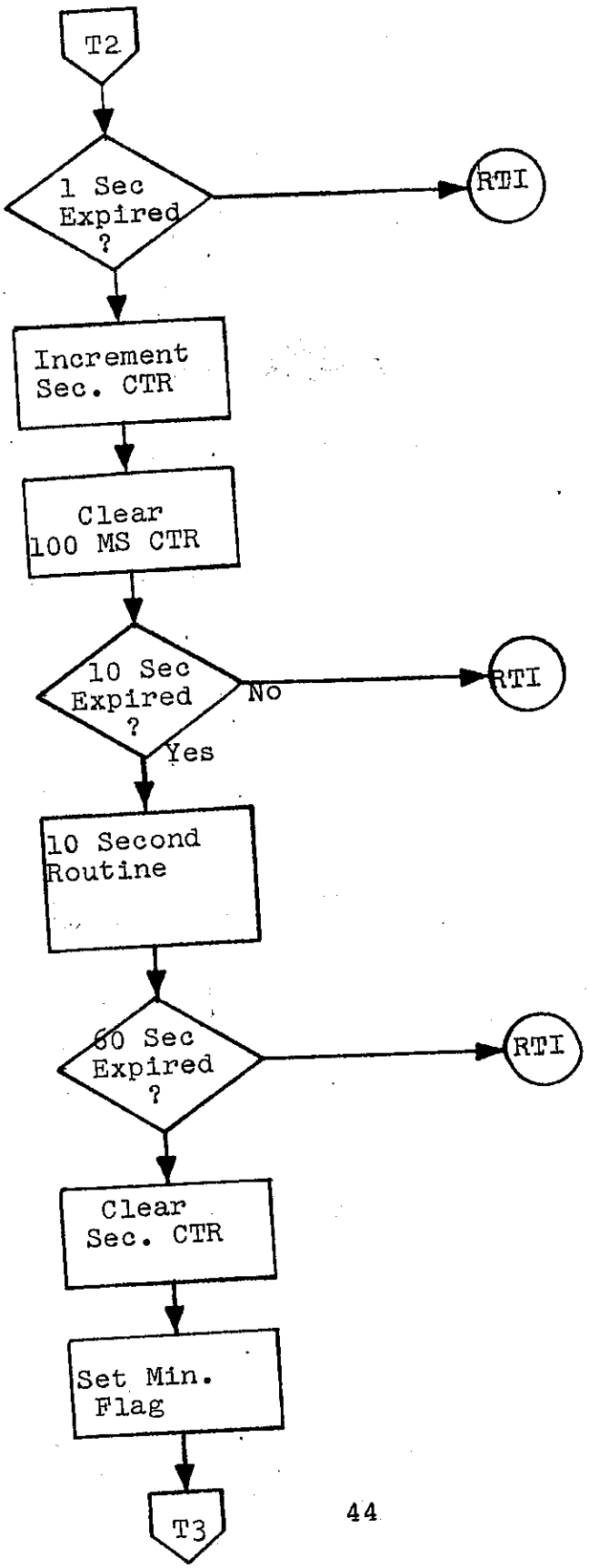
TIME SERVICE



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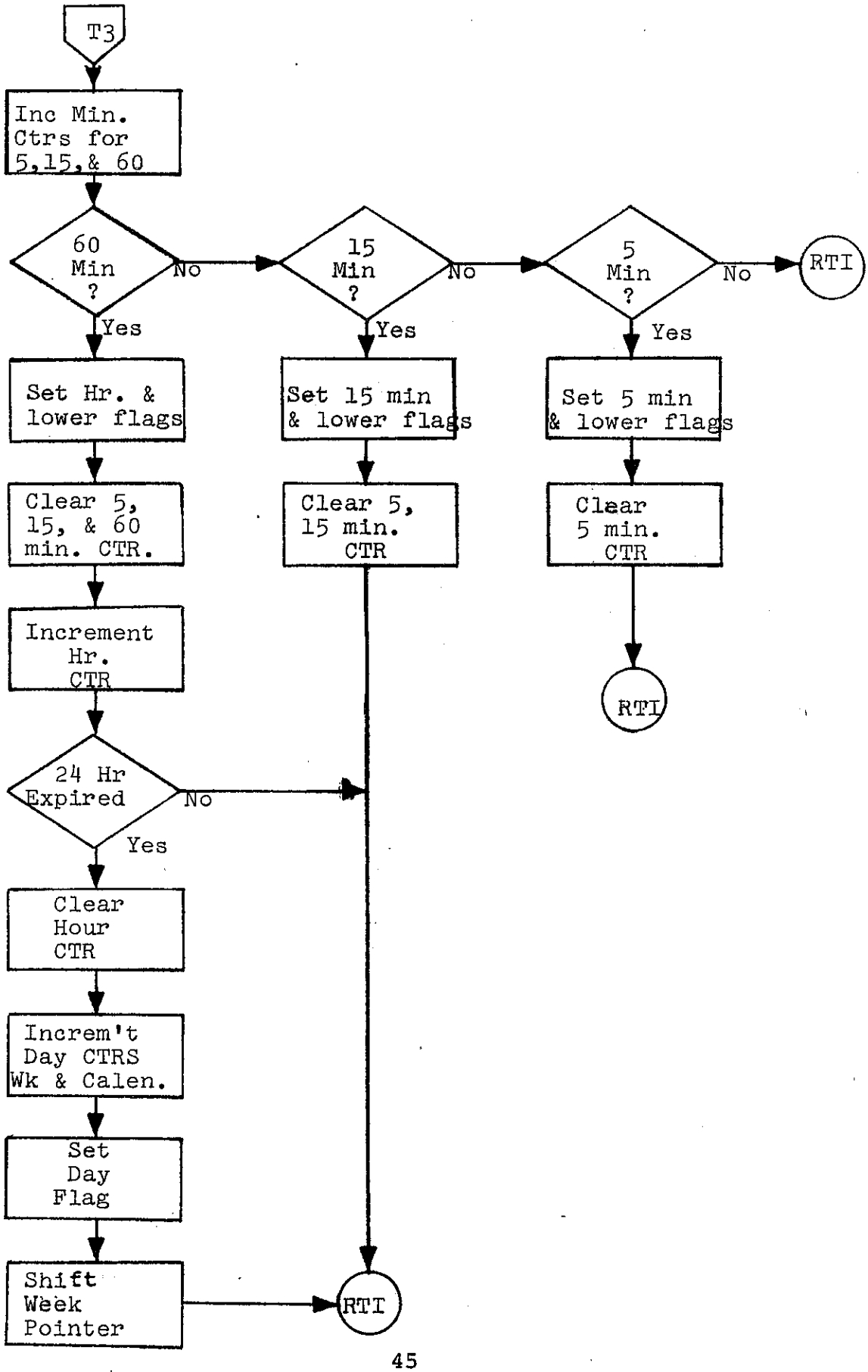
TIME SERVICE



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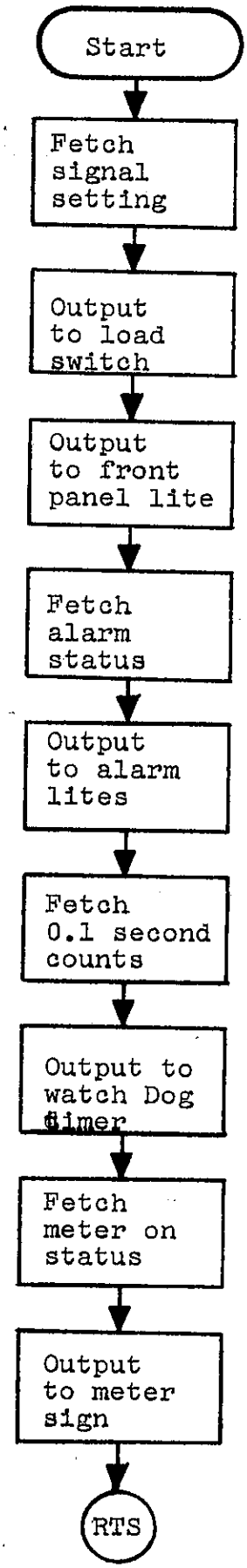
SIGNALS AND SIGN OUTPUTS



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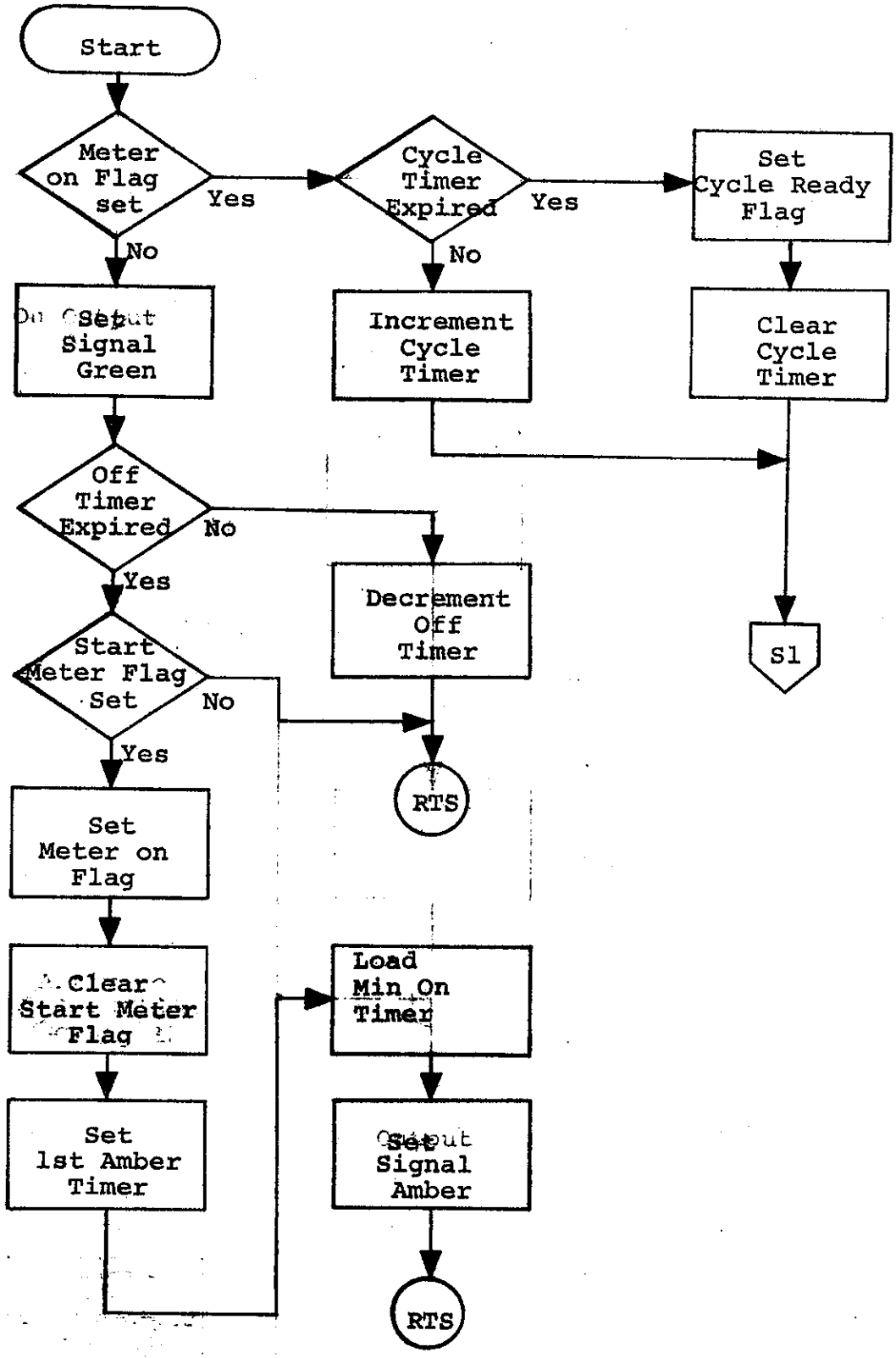

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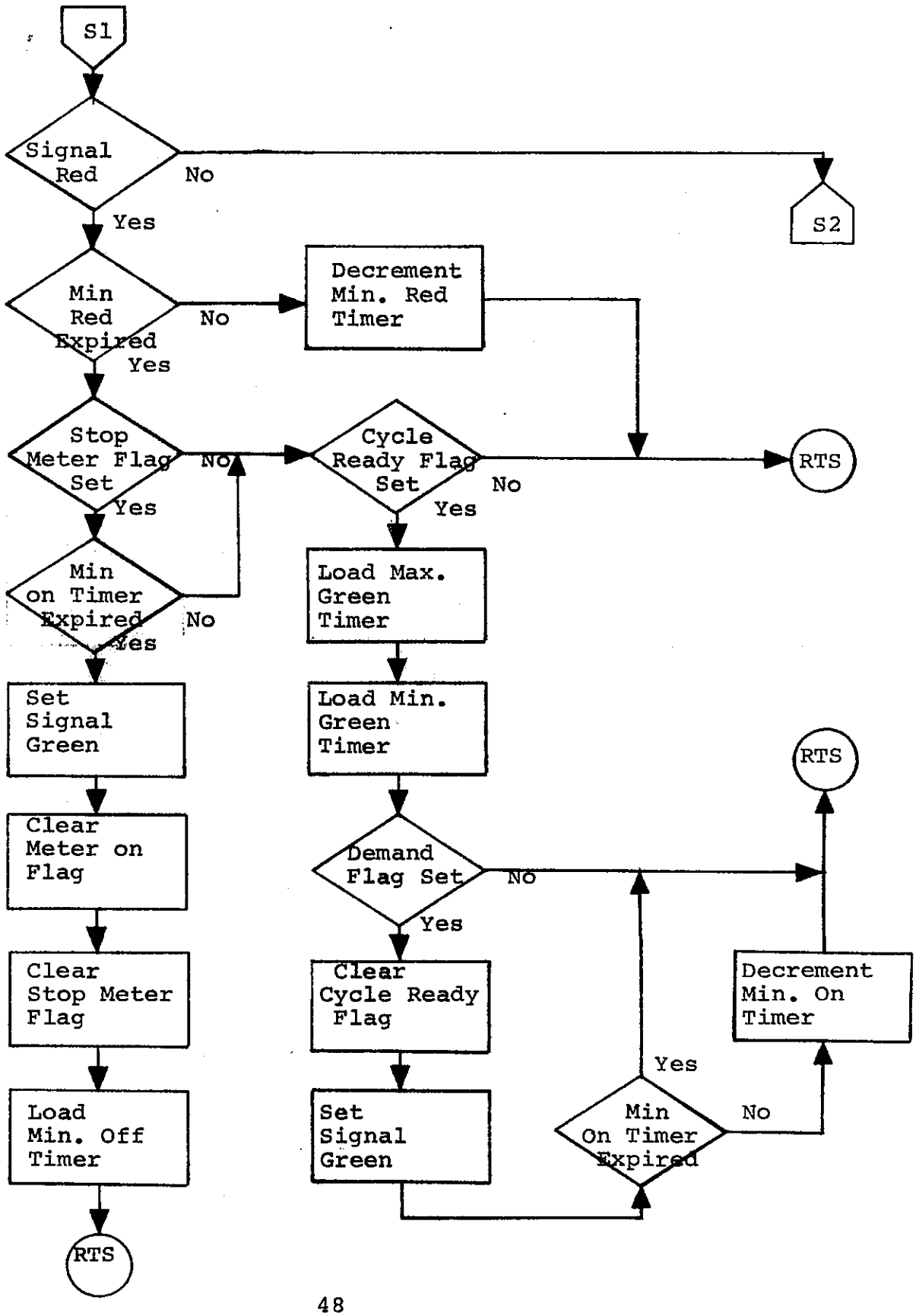

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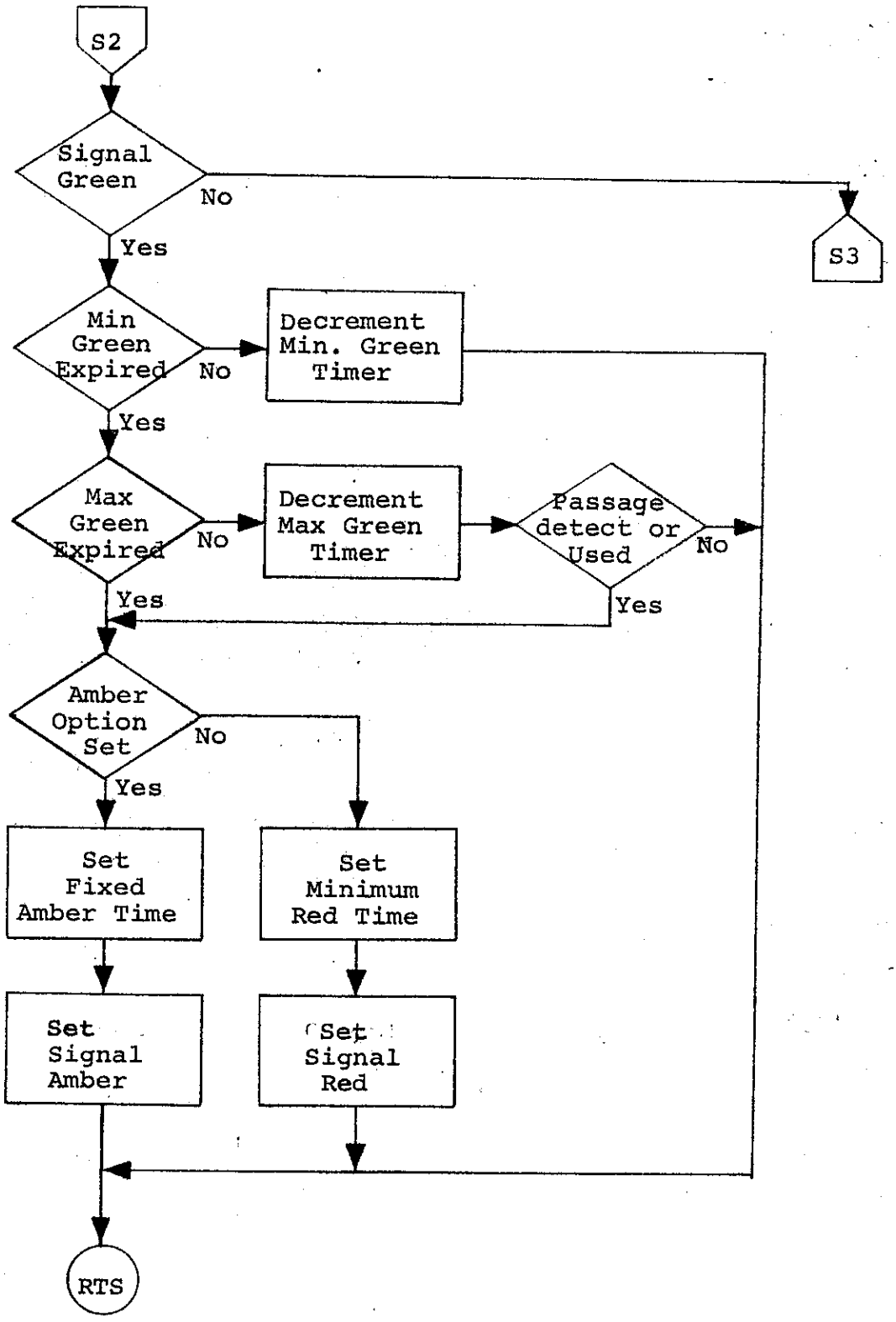

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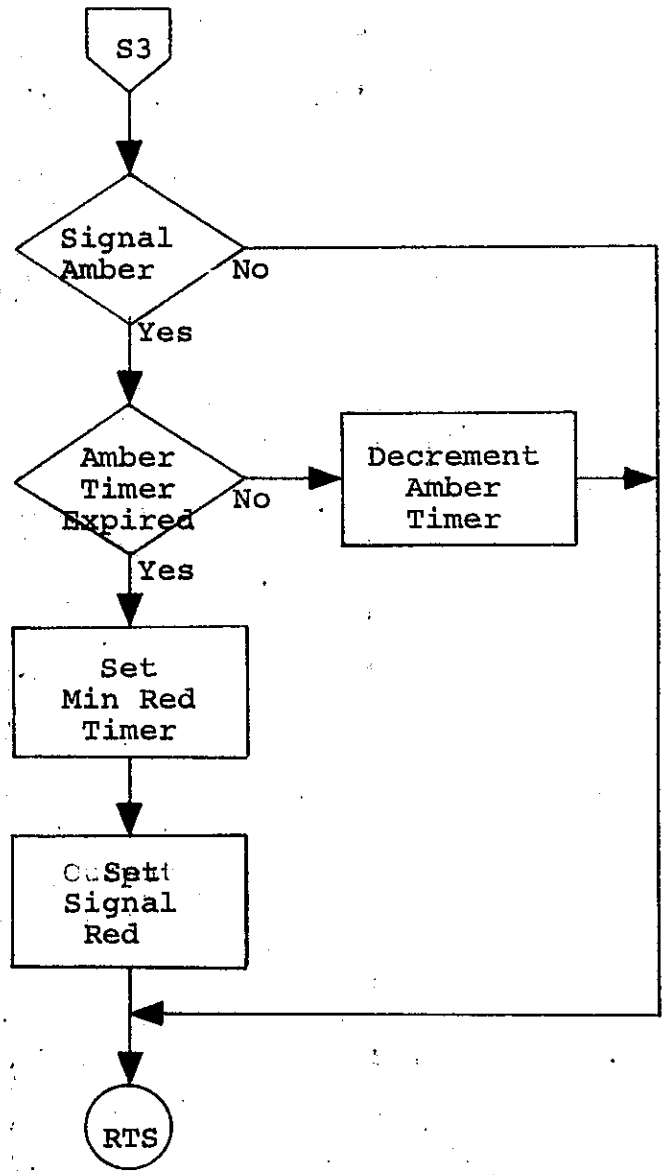

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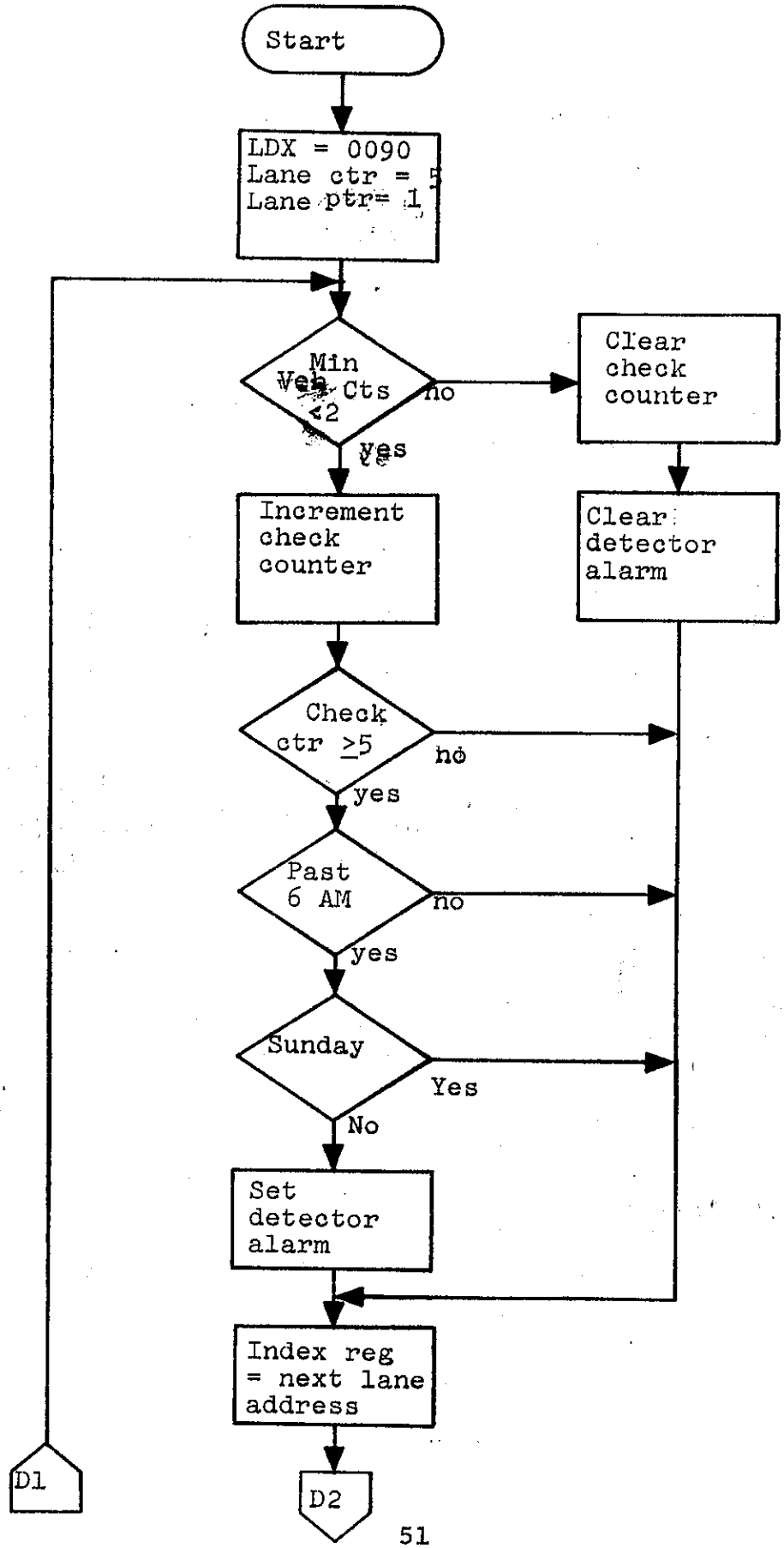
DETECTOR CHECKS



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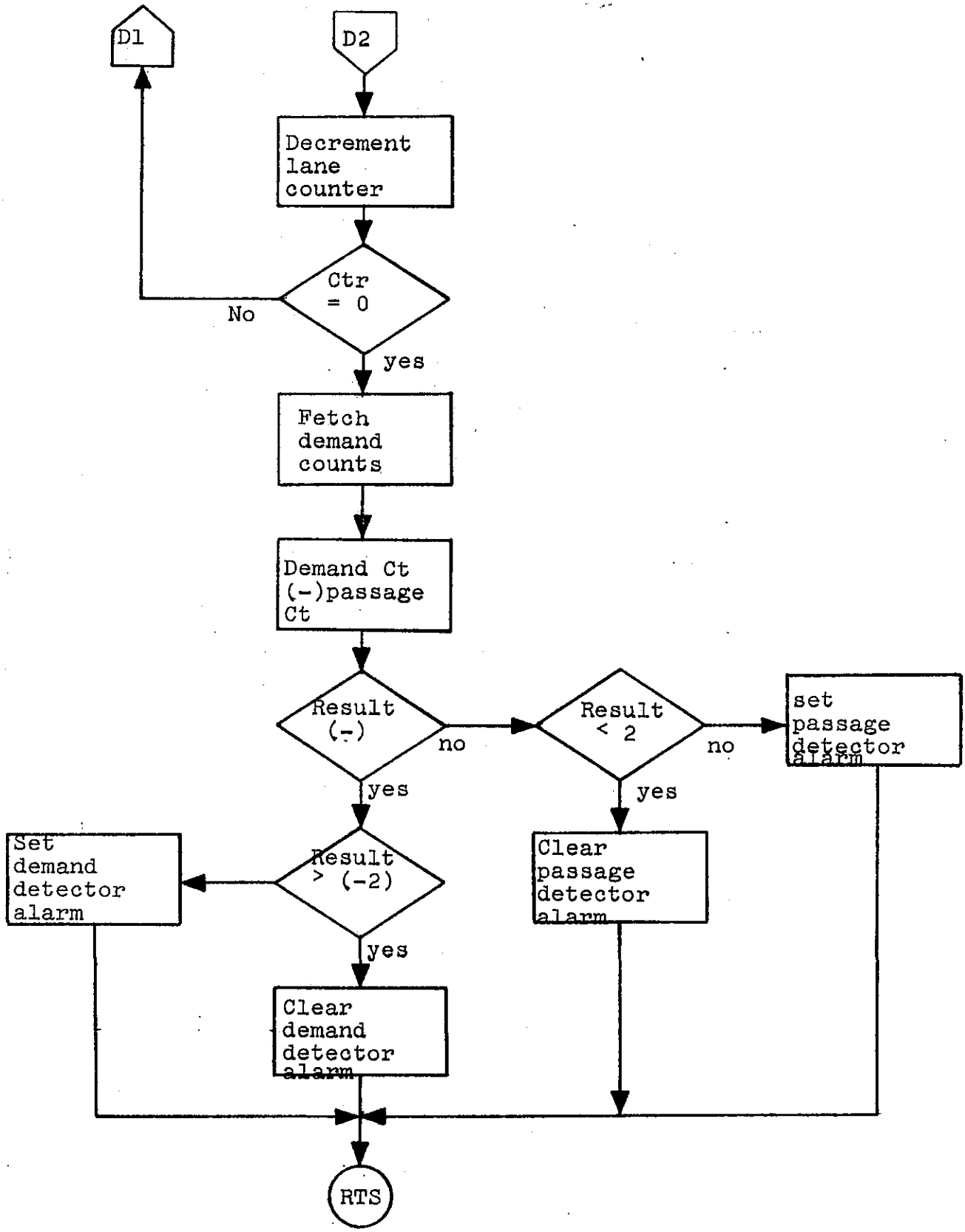
DETECTOR CHECKS



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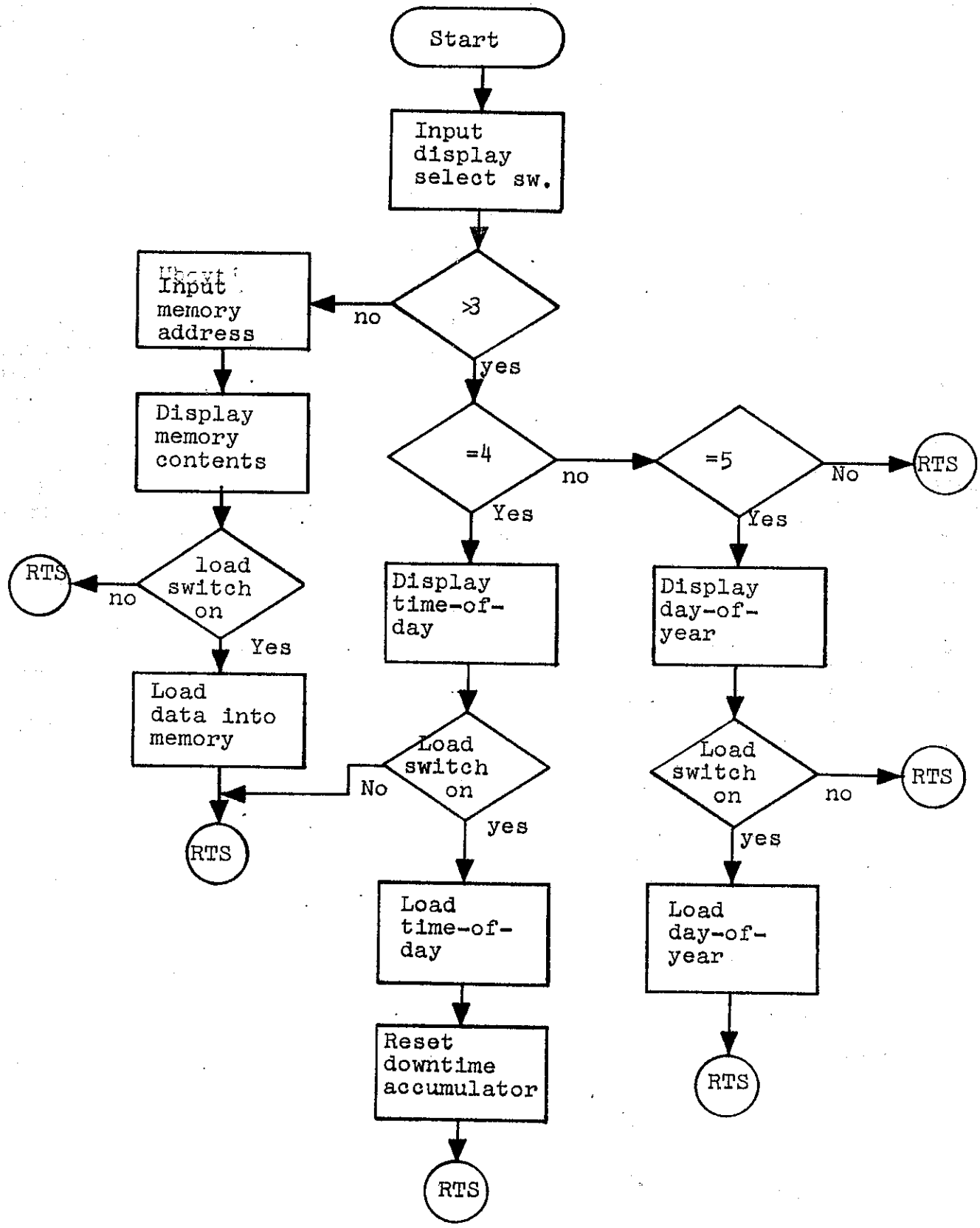

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POWER ON/RESET

ADDRESS	OPER CODE	OPERAND		LABEL	MNEM.		COMMENTS
39F8	8E	01	7F		LDS	017F	Set stack pointer
B	7F	00	FB		CLR	00FB	Clear 00FB
E	7F	00	FF		CLR	00FF	Clear 00FF
3A01	86	C0			LDAA	#C0	
3	97	FC			STAA	FC	00FC = C0
5	86	FF			LDAA	#FF	
7	97	50			STAA	50	Ramp detectors [illegible]
9	97	51			STAA	51	M.L. detectors [illegible]
B	01				NOP		
C	01				NOP		
D	01				NOP		
E	01				NOP		
F	01				NOP		
3A10	B6	10	00		LDAA	1000	A=power down time
3	97	00			STAA	00	Store down time
5	27	1D			BEQ	GRNS	Set signal green
7	81	FF			CMPA	#FF	Downtime ≥ 256 min
9	26	0A			BNE	CTDN	
B	86	01			LDAA	#01	Yes,
D	B7	01	32		STAA	NMFG	Set NO Meter Flag
3A20	B7	10	05		STAA	1005	Alarm lite #1 on
3	20	0F			BRA	GRNS	Set Signal Green
5	7A	00	00	CTDN	DEC	0000	Downtime -1
8	CE	01	00		LDX	#0100	I.R = 0100
B	3F				SWI	384A	TOD + 1 min
C	96	00			LDAA	00	
E	26	F5			BNE	CTDN	Downtime = 0?
3A30	4F				CLRA		A = 0
1	B7	10	00		STAA	1000	Clear downtime [illegible]
4	86	80		GRNS	LDAA	#80	
6	B7	01	4F		STAA	014F	Set signal green
9	BD	3B	F1		JSR		Meter rate selecti[illegible]

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ADDRESS	OPER CODE	OPERAND		LABEL	MNEM.		COMMENTS
3A3C	B6	01	54	FLAG	LDAA	0154	Fetch time flag
F	84	03			ANDA	#03	50 ms or 100 ms fl
3A41	27	F9			BEQ	FLAG	Branch back if neit
3	85	02			BITA	#02	100 ms flag set?
5	27	03			BEQ	DTSR	
7	BD	3C	DB		JSR	SIGNAL	Signal Service
A	BD	3A	70	DTSR	JSR	DTSR	Detector Service
D	86	FC			LDAA	#FC	
F	B4	01	54		ANDA	0154	Clear 50&100 ms flag
3A52	B7	01	54		STAA	0154	Restore time flag
5	BD	3B	F1		JSR	RATE	Rate Selection
8	BD	3C	AF		JSR	OUTSN	Signal & Sign Output
B	BD	3A	BB		JSR	VEHC	Vehicle Count
E	BD	3B	3A		JSR	DETC	Detectors check
3A61	BD	3B	A2		JSR	3MIN	3 Min Occupancy
4	BD	3D	9C		JSR	CONSO	Console Service
7	7E	3A	3C		JMP	FLAG	Return

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OCCUPANCY COMPUTATION & DETECTOR CHECKING

ADDRESS	OPER CODE	OPERAND		LABEL	MNEM.		COMMENTS
38E0	86	05			LDAA	#05	
2	97	0A			STAA	0A	Set lane ptr = 5
4	7C	00	FF		INC	00FF	Inc 10 sec ptr
7	86	07			LDAA	#07	
9	B1	00	FF		CMPA	FF	60 sec expired
C	26	0A			BNE	INCP	
E	86	00			LDAA	#00	Reset 10 Sec ptr = 1
38F0	97	FF			STAA	FF	
2	86	C0			LDAA	#C0	Reset ctr ptr = C0
4	97	FC			STAA	FC	
6	20	03			BRA	LDXP	
8	7C	00	FC	INCP	INC	00FC	Inc Ctr Ptr
	-	-					
B	DE	FB		LDXP	LDX	FB	Set Ctr Ptr in Index
D	6F	00			CLR	,00	Clr Occup Ctr
F	86	0B			LDAA	#0B	
3901	9B	FC			ADDA	FC	Advaire ctr ptr to
3	97	FC			STAA	FC	next lane
5	7A	00	0A		DEC	000A	Dec lane ctr
8	26	F1			BNE	LDXP	
A	86	C9			LDAA	#C9	
C	9B	FC			ADDA	FC	Rturn ctr ptr to lane #1
E	97	FC			STAA	FC	
3910	86	C0			LDAA	#C0	
2	7F	00	06		CLR	0006	Set starting ptr=C0
5	97	07			STAA	07	
7	7F	00	04		CLR	0004	
A	86	C7			LDAA	#C7	
C	97	05			STAA	05	Set sum ptr = C7
E	86	05			LDAA	#05	
3920	97	0A			STAA	0A	Set lane ptr
2	86	06		LDXL	LDAA	#06	
4	97	0B			STAA	03	Set 10 sec loop ctr=6
6	DE	06			LDX	06	
8	C6	00			LDAB	#00	
A	A6	00			LDAA	,00	A = 00C0 content
C	AB	01		ADD	ADDA	,01	A = 00C0 + 00C1
E	C9	00			ADCB	#00	B = C+0
3930	08				INX		IR = IR+1
1	7A	00	0B		DEC	000B	10 sec counter -1
4	26	F6			BNE	ADD	
6	DE	04			LDX	04	IR = Sum address
8	A7	00			STAA	,00	Store Sum, LSB
A	E7	01			STAB	,01	Store Sum, MSB
C	B7	00	1B		STAA	001B	Store dividend LSB
F	F7	00	1A		STAB	001A	Store dividend MSB
3942	86	0C			LDAA	#0C	Divisor = 12
4	B7	00	19		STAA	0019	
7	BD	39	B6		JSR	DIVIDE	Division subroutine
A	96	1D			LDAA	1D	

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OCCUPANCY COMPUTATION & DETECTOR CHECKS (Continued)

ADDRESS	OPER CODE	OPERAND		LABEL	MNEM.		COMMENTS
C	A7	0D			STAA	,0D	Store total next lane
E	7D	00	0D		TST	000D	
3951	26	04			BNE	DBE	Ave lane Occup
3	91	0C			CMPA	0C	than 2 (ML Occup)?
5	2E	0E			BGT	BAD	
7	AB	0D		DBE	ADDA	,0D	Ave lane Occ than
9	25	04			BCS	GOOD	1/2 (Ave ML OCC)?
B	91	F9			CMPA	F9	
D	2D	06			BLT	BAD	
F	A6	0D		Good	LDAA	,0D	
3961	A7	02		STAO	STAA	,02	Store Ave lane occup
3	20	0A			BRA	NLNE	
5	86	05		BAD	LDAA	#05	
7	91	0A			CMPA	0A	1st lane?
9	26	04			BNE	NLNE	
B	96	DF			LDAA	DF	Use 3rd in Ave Occup
D	A7	02			STAA	,02	
F	7A	00	0A	NLNE	DEC	000A	Dec LN Ptr
3972	27	0E			BEQ	MLOT	
4	86	0B			LDAA	#0B	Advance Ctr Ptr
6	9B	07			ADDA	07	
8	97	07			STAA	07	
A	86	0B			LDAA	#0B	Advance Sum Ptr
C	93	05			ADDA	05	
E	97	05			STAA	05	
3980	20	A0			BRA	LDXL	
2	96	C7		MLOT	LDAA	C7	
4	D6	C8			LDAB	C8	
6	9B	D2			ADDA	D2	Add 1st&2nd lane occu
8	D9	D3			ADCB	D3	
A	9B	DD			ADDA	DD	Add 3rd lane occup
C	D9	DE			ADCB	DE	
E	9B	E8			ADDA	E8	Add 4th lane occup
3990	D9	E9			ADCB	E9	
2	9B	F3			ADDA	F3	Add 5th lane occup

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Occupancy Computation & Detector Checks (Continued)

ADDRESS	OPER CODE	OPERAND	LABEL	MNEM.		COMMENTS
3994	D9	F4		ADCB	F4	
6	97	F7		STAA	F7	00F7=ML occup Count
8	D7	F8		STAB	F8	
A	97	1B		STAA	1B	Set dividend LSB
C	D7	1A		STAB	1A	Set dividend MSB
E	86	3C		LDAA	#3C	Divisor = 60
0	97	19		STAA	19	
2	BD	39	B6	JSR	Divide	Division Subroutine
5	96	1D		LDAA	1D	
7	97	F9		STAA	F9	ML Ave Occup (%)
9	9B	F9		ADDA	F9	2 (% Occup)
B	5F			CLRB		
C	C9	00		ADCB	#00	
E	D7	0D		STAB	0D	Store
0	97	0C		STAA	0C	
2	CE	01	00	LDX	0100	IR = 0100
5	39			RTS		

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ADDRESS	OPER CODE	OPERAND		LABEL	MNEM.		COMMENTS
39B6	C6	08			LDAB	#8	S = 8
8	7F	00	1C		CLR	001C	
B	7F	00	1D		CLR	001D	
E	5C			DVPO	INCB		S = S+1
F	C1	10			CMPB	#10	S > 16
39C1	2E	34			BGT	RTS	
3	78	00	19		ASL		Shift Divisor Left 1
6	24	F6			BCC	DVPO	
8	D7	1E			STAB		Store justified div.
A	76	00	19		ROR		Shift divisor back 1
D	96	1A			LDAA		Load A Dividend
F	91	19		DVP1	CMPA	19	
39D1	25	0D			BCS	DVSU	Divisor
3	0D			DVP2	SEC		If Dividend _ Divisor
4	79	00	1D		ROL		Shift Quotient left 1
7	79	00	1C		ROL		
A	90	19			SUBA	19	Dividend -Divisor
C	97	1A			STAA	1A	Store New Dividend
E	20	07			BRA	DVSH	
39E0	0C			DVSU	CLC		
1	79	00	1D		ROL		Shift Quotient Left
4	79	00	1C		ROL		
7	5A			DVSH	DECB		S = S-1
8	27	0D			BEQ	RTS	Stop if S = 0
A	0C				CLC		If S 0, Shift Dividen
B	79	00	1B		ROL		left 1 bit, LSB=0
E	79	00	1A		ROL		
39F1	96	1A			LDAA		
3	25	DE			BCS		
5	20	D8			BRA		
7	39				RTS		

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3-Minute Occupancy Computation

ADDRESS	OPER CODE	OPERAND	LABEL	MNEM.		COMMENTS
3BA2	96	8C		LDAA	8C	Min expired?
4	26	01		BNE	01	
6	39			RTS		
7	7F	00	8C	CLR	008C	
A	86	80		LDAA	#80	Address = 80+ pointer
C	9B	8F		ADDA	8F	
E	97	8E		STAA	8E	
3BB0	7F	00	8D	CLR	008D	
3	DE	8D		LDX	8D	I.R. = Address
5	96	F7		LDAA	F7	Fetch 1 min occup
7	A7	00		STAA	,00	Store " "
9	96	F8		LDAA	F8	
B	A7	01		STAA	,01	
D	7C	00	8F	INC	008F	Pointer +2
3BC0	7C	00	8F	INC	008F	
3	86	06		LDAA	#06	A = 6
5	91	8F		CMPA	8F	A - Pointer
7	2C	03		BGE	03	
9	7F	00	8F	CLR	008F	Pointer = 0
C	CE	00	80	LDX	0080	I.R. = 0080
F	C6	00		LDAB	#00	B = 0
3BD1	A6	00		LDAA	,00	
3	AB	02		ADDA	,02	A = 80+82+84
5	E9	01		ADCB	,01	B = 81+83+85+C
7	EB	03		ADDB	,03	
9	AB	04		ADDA	,04	
B	E9	05		ADCB	,05	
D	A7	06		STAA	,06	Store A, LSB SUM
F	E7	07		STAB	,07	" B, MSB SUM
3BE1	97	1B		STAA	1B	A = LSB dividend
3	D7	1A		STAB	1A	B = MSB "
5	86	B4		LDAA	#B4	Divisor = 180
7	97	19		STAA	19	
9	BD	39	B6	JSR	Divide	Division routine
C	96	1D		LDAA	1D	A = % occupancy
E	97	88		STAA	88	Store % occupancy
3BF0	39			RTS		

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Meter Rate Selection

ADDRESS	OPER CODE	OPERAND		LABEL	MNEM.		COMMENTS
3BF1	CE	00	60		LDX	#0060	
4	B6	01	5D	LSB	LDAA	015D	
7	A1	00			CMPA	,00	
9	27	0E			BEQ	MSB	
B	08				INX		
C	08				INX		
D	8C	00	80		CPX	#0080	
3C00	26	F2			BNE	LSB	
2	CE	01	30	CLRF	LDX	0130	
5	6F	02			CLR	,02	
7	20	14			BRA	SWIN	
9	B6	01	5E	MSB	LDAA	015E	
C	A1	01			CMPA	,01	
E	26	F2			BNE	CLRF	
3C10	CE	01	30		LDX	0130	
3	6C	02			INC	,02	
3C15	96	00			LDAA	,00	Meter on flag status?
7	26	01			BNE	01	Clear flag if set.
9	39				RTS		
A	6F	00			CLR	,00	Clear meter on flag.
C	39				RTS		
D	B6	10	04	SWIN	LDAA	1004	Input mode switch.
3C20	84	40			ANDA	#40	Switch on manual?
2	27	0F			BEQ	FITR	No, to fixed time.
4	B6	10	04		LDAA	1004	Input manual rate.
7	8D	4D			BSR	FCON	To fixed rate convert.
9	96	00			LDAA	,00	Meter on flag status?
B	27	01			BEQ	01	
D	39				RTS		
E	86	01			LDAA	#01	Set start meter flag.
3C30	97	01			STAA	,01	
2	39				RTS		
3	C6	20		FITR	LDAB	#20	Begin fixed time rate search.
5	CE	01	80		LDX	#180	Set IR = 0180.
8	B6	01	5B	MISH	LDAA	015B	Get TOD hour.
B	A1	00			CMPA	,00	Compare hour.
D	26	12			BNE	12	No. branch.
F	B6	01	5A		LDAA	015A	Get TOD minute.
3C42	A1	01			CMPA	,01	Compare minute.
4	26	0B			BNE	0B	
6	B6	01	5F		LDAA	015F	Get TOD day of week.
9	A4	02			ANDA	,02	Compare day of week.
B	27	04			BEQ	04	
D	A6	03			LDAA	,03	
F	20	08			BRA	Action	

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Meter Rate Selection

ADDRESS	OPER CODE	OPERAND		LABEL	MNEM.		COMMENTS
3C51	08				INX		IR + 1
2	08				INX		IR + 1
3	08				INX		IR + 1
4	08				INX		IR + 1
5	5A				DECB		DEC loop counter.
6	26	E0			BNE	MISH	Zero? No, branch back.
8	39				RTS		Yes, return.
9	84	F0		Action	ANDA	#F0	Get transition type.
B	81	F0			CMPA	#F0	Is it F?
D	26	07			BNE	07	No. branch.
F	7C	01	31		INC	0131	Set start meter flag.
2	A6	03			LDAA	,03	Get meter rate code.
4	20	10			BRA	FCON	Conversion code.
6	81	E0			CMPA	#E0	Is it E?
8	26	04			BNE	04	No, branch.
A	A6	03			LDAA	03	Get meter rate.
C	20	08			BRA	FCON	To rate conversion.
E	81	D0			CMPA	#D0	Is it D?
3C70	26	16			BNE	TRME	No, to traffic responsive.
2	7C	01	3E	Stop	INC	013E	Yes, set stop meter flag.
5	39				RTS		
6	84	0E		FCON	ANDA	#0F	Clear prefix.
8	CE	01	20		LDX	#120	IR = 0120
B	4D				TSTA		Acc. A = 0?
C	27	04			BEQ	04	Yes, branch.
E	08				INX		IR = IR + 1
F	4A				DECA		A = A - 1
3C80	20	F9			BRA	F9	Branch back.
2	A6	00			LDAA	,00	
4	B7	01	38		STAA	0183	Set cycle time.
7	39				RTS		
8	96	88		TRME	LDAA	88	Fetch 3-min occup.
A	91	89			CMPA	89	Compare with threshold.
C	2C	02			BGE	RCON	If ≥ than threshold.
E	20	E2			BRA	Stop	If <, set stop meter flag.
3C90	86	01		RCON	LDAA	#01	Begin rate search.
2	97	0E			STAA	0E	Rate address = 0120.
4	86	20			LDAA	#20	
6	97	0F			STAA	#0F	
8	CE	01	10		LDX	#0110	IR = 0110
B	D6	F9			LDAB	F9	Fetch latest min occup.
D	E1	00		CMPR	CMPB	,00	Compare with threshold.
F	2F	06			BLE	CYTE	Match if ≤ threshold.

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Meter Rate Selection

ADDRESS	OPER CODE	OPERAND		LABEL	MNEM.		COMMENTS
3CA1	08				INX		IR = X + 1
2	7C	00	0F		INC	000F	Rate address + 1
5	20	F6			BRA	CMPR	
7	DE	0E		CYTE	LDX	0E	IR = Address of rate
9	A6	00			LDA	,00	Fetch rate (cycle time).
B	B7	01	38		STAA	0138	Store cycle time.
E	39				RTS		

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DETECTOR SERVICE

ADDRESS	OPER CODE	OPERAND	LABEL	MNEM.		COMMENTS
3A70	C6	05		LDAB	#05	Lane Ctr = 5
2	D7	02		STAB	02	Detectors used
4	D6	51		LDAB	51	
6	01	01		NOP		
8	B6	10	01	LDAA	1001	Load detectors
B	94	51		ANDA	51	Verify with preset units
D	97	53		STAA	53	
F	DE	FB	ADDR	LDX	FB	LDX starting address check for presence
3A81	44			LSRA		
2	24	02		BCC	ADV	
4	6C	00		INC	,00	Inc occupancy ctr
6	C6	0B	ADV	LDAB	#0B	Set ctr address for next m. lane
8	DB	FC		ADDB	FC	
A	D7	FC		STAB	FC	
C	7A	00	02	DEC	0002	Decrement lane ctr
F	26	EE		BNE	ADDR	Repeat for all 5lanes
3A91	C6	C0		LDAB	#C0	
3	DB	FF		ADDB	FF	
5	D7	FC		STAB	FC	FC=Next starting addr
7	96	50	RAMP	LDAA	50	A=ramp detector used
9	B4	10	02	ANDA	1002	Verify
C	85	01		BITA	#01	Test demand
E	27	07		BEQ	07	if not, clear flag
3AA0	C6	01		LDAB	#01	
2	F7	01	43	STAB	0143	Clear demand flag
5	20	03		BRA	PASS	
7	7F	01	43	CLR	0143	Clear demand flag
A	85	02	PASS	BITA	#02	Test passage
C	27	07		BEQ	07	if not, clear flag
E	C6	01		LDAB	#01	
3AB0	F7	01	44	STAB	0144	Set passage flag
3	20	03		BRA	RTS	
5	7F	01	44	CLR	0144	Clear passage flag
8	97	52		STAA	52	Store ramp detector
A	39			RTS		

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VEHICLE COUNT

ADDRESS	OPER CODE	OPERAND		LABEL	MNEM.		COMMENTS
3ABB	86	05			LDAA	#05	
D	97	02			STAA	02	M.lane Ctr = 05
F	86	02			LDAA	#02	
3AC1	97	03			STAA	03	ML/Ramp Ctr=02
3	CE	00	20		LDX	0020	IR=Starting Address
6	D6	53			LDAB	53	
8	54			BIT	LSRB		Presence?
9	24	14			BCC	GAP	
B	6F	01			CLR	,01	gap counter = 0
D	6C	00			INC	,00	presence ctr +1
F	86	02			LDAA	#02	
3AD1	A1	00			CMPA	,00	Presence Ctr = 2 ?
3	26	08			BNE	NLAN	
5	6D	02			TST	,02	Gap Flag set?
7	27	04			BEQ	NLAN	
9	6F	02			CLR	,02	Clear Gap Flag
B	6C	70			INC	,70	Vehicle Counter +1
D	20	10			BRA	NLAN	
F	6F	00		GAP	CLR	,00	Clear Presence Ctr
3AE1	6D	02			TST	,02	Gap Flag set?
3	26	OA			BNE	NLAN	
5	6C	01			INC	,01	Gap Counter +1
7	86	05			LDAA	#05	
9	A1	01			CMPA	,01	Gap Counter = 5?
B	26	02			BNE	NLAN	
D	6C	02			INC	,02	Set Gap Flag
F	08			NLAN	INX		I.R.+3
3AF0	08				INX		
1	08				INX		
2	7A	00	02		DEC	0002	Lane Ctr - 1
5	26	D1			BNE	BIT	All lanes checked?
7	7A	00	03		DEC	0003	
A	27	0B			BEQ	TOTAL	
C	86	03		RAMP	LDAA	#03	
E	97	02			STAA	02	Set ramp lanes = 3
3B00	CE	00	41		LDX	0041	IR = 0040
3	D6	52			LDAB	52	Load ramp detectors
5	20	C1			BRA	BIT	
7	86	04		TOTAL	LDAA	#04	
9	B4	01	54		ANDA	0154	Min flag set ?
C	26	01			BNE	01	
E	39				RTS		
F	84	FB			ANDA	#FB	Clear min flag
3B11	B7	01	54		STAA	0154	
4	CE	00	90		LDX	0090	IR = 0090
7	86	OE			LDAA	#OE	
9	97	02			STAA	02	Lane ctr = OE
B	7F	00	BF		CLR	00BF	Clear ML total ctr
E	A6	00		FETCH	LDAA	,00	Fetch count

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ADDRESS	OPER CODE	OPERAND		LABEL	MNEM.		COMMENTS
3B20	A7	01			STAA	,01	Store lane total
2	6F	00			CLR	,00	Clear counter
4	C6	09			LDAB	#09	A = 09
6	D1	02			CMPB	02	Loop through 5 ML ?
8	2C	04			BGE	04	
A	9B	BF			ADDA	BF	Total lane counts
C	97	BF			STAA	BF	Store ML total
E	08				INX		IR + 1
F	08				INX		IR + 1
3B30	08				INX		IR + 1
1	7A	00	02		DEC	0002	Lane Ctr - 1
4	26	E8			BNE	FETCH	Repeat for next lane
6	7C	00	8C		INC	008C	Set flag
9	39				RTS		

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ADDRESS	OPER CODE	OPERAND	LABEL	MNEM.		COMMENTS
3800	B6	10	0B	LDAA	100B	Read Pwr fail input
3	84	01		ANDA	#01	
5	27	01		BEQ	Clock	
7	3E			WAI		
8	CE	01	00	LDX	0100	Store registers
B	6C	55	Clock	INC	,55	
D	86	03		LDAA	#03	Inc 60 ctr
F	A1	55		CMPA	,55	
3811	26	08		BNE	HUN	50 MS?
3	86	01		LDAA	#01	
5	AA	54		ORAA	,54	
7	A7	54		STAA	,54	Set 50 MS flag
9	20	16		BRA	RTI	
B	86	06		LDAA	#06	
D	A1	55		CMPA	,55	
F	26	10		BNE	RTI1	100 MS?
3821	86	03		LDAA	#03	
3	AA	54		ORAA	,54	Set 50 & 100 MS flags
5	A7	54		STAA	,54	
7	6F	55		CLR	,55	
9	6C	56		INC	,56	Clr 60 ctr
B	86	0A		LDAA	#0A	INC 100 M.S. Ctr
D	A1	56		CMPA	,56	
F	27	01		BEQ	SEC	
3831	3B		RTI1	RTI		
2	6F	56		CLR	,56	
4	86	01		LDAA	#01	Clr 100 MS Ctr
6	AB	57		ADDA	,57	
8	19			DAA		INC 1 Sec Ctr
9	A7	57		STAA	,57	
B	84	0F		ANDA	#0F	
D	01	09		NOP		Check for 10 sec intervals, LSB=0
E	26	38	E0	BNE	RT12	
3840	BD	60		JSR	OCCU	To Occup. Update
3	86	57		LDAA	#60	
5	A1	01		CMPA	,57	
7	27			BEQ	MIN	
9	3B	04	RTI2	RTI		
A	86	54	Min	LDAA	#04	
C	AA	54		ORAA	,54	Set Min Flag
E	A7	57		STAA	,54	
3850	6F	58		CLR	,57	
2	6C	59		INC	,58	Clear Sec. Ctr
4	6C	01		INC	,59	Inc 5 Min Ctr
6	86			LDAA	#01	Inc 15 Min Ctr

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TIME SERVICE (Continued)

ADDRESS	OPER CODE	OPERAND	LABEL	MNEM.		COMMENTS
3858	AB	5A		ADDA	,5A	Inc 60 Min Ctr
A	19			DAA		
B	C6	60		LDAB	#60	60 min expired?
D	11			CBA		
E	27	22		BEQ	HRF	Restore if ≠ 60
60	A7	5A		STAA	,5A	
2	86	0F		LDAA	#0F	15 min expired?
4	A1	59		CMPA	,59	
6	27	0F		BEQ	FMF	
8	86	05		LDAA	#05	5 min expired?
A	A1	58		CMPA	,58	
C	26	08		BNE	RT1	Set 5 min flags
E	86	0F		LDAA	#0F	
3870	AA	54		ORAA	,54	
2	A7	54		STAA	,54	Clr 5 min ctr.
4	6F	58		CLR	,58	
6	3B		RTI	RTI		
7	86	1F	FMF	LDAA	#1F	Set 15 min & lower flags
9	AA	54		ORAA	,54	
B	A7	54		STAA	,54	
D	6F	58		CLR	,58	Clr 5 min ctr
F	6F	59		CLR	,59	Clr 15 min ctr
3881	3B			RTI		
2	86	3F	HRF	LDAA	#3F	Set HR &Lower Flags
4	AA	54		ORAA	,54	
6	A7	54		STAA	,54	
8	6F	58		CLR	,58	Clr 5 min ctr
A	6F	59		CLR	,59	Clr 15 min ctr
C	6F	5A		CLR	,5A	Clr 60 min ctr
E	01			NOP		
F	86	01		LDAA	#01	Inc Hr Ctr
3891	AB	5B		ADDA	,5B	
3	19			DAA		
4	C6	24		LDAB	#24	24 hr. Expired?
6	11			CBA		
7	27	03		BEQ	03	
9	A7	5B		STAA	,5B	Restore if ≠ 0
B	3B			RTI		
C	6F	5B		CLR	,5B	Clr Hr. flag
E	86	7F		LDAA	#7F	

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ADDRESS	OPER CODE	OPERAND	LABEL	MNEM.		COMMENTS
38A0	A7	54		STAA	,54	Set day flag
2	6C	5C		INC	,5C	Inc day counter
4	86	08		LDAA	#08	
6	A1	5C		CMPA	,5C	Week expired?
8	27	04		BEQ	SUN	RTN to Sunday (01)
A	68	5F		ASL	,5F	Shift week ptr
C	20	06		BRA	06	
E	86	01	SUN	LDAA	#01	
38B0	A7	5C		STAA	,5C	Reset to Sunday
2	A7	5F		STAA	,5F	Reset ptr to Sunday
4	86	01		LDAA	#01	
6	AB	5D		ADDA	,5D	INC Julian Calender
8	19			DAA		LSB dec. adjust
9	A7	5D		STAA	,5D	
B	25	02		BCS	MSB	Carry to MSB
D	20	07		BRA	,07	
F	86	01	MSB	LDAA	#01	
38C1	AB	5E		ADDA	,5E	Inc MSB Calender
3	19			DAA		
4	A7	5E		STAA	,5E	
6	86	03		LDAA	#03	Reset calender if=366
8	A1	5E		CMPA	,5E	
A	26	0C		BNE	RTI3	
C	86	66		LDAA	#66	
E	A1	5D		CMPA	,5D	
38D0	26	06		BNE	RTI3	
2	6F	5E		CLR	,5E	
4	86	01		LDAA	#01	
6	A7	5D		STAA	,5D	
8	3B		RTI3	RTI		

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Signals and Sign Outputs

ADDRESS	OPER CODE	OPERAND		LABEL	MNEM.		COMMENTS
					LDX	0100	IR = 0100
3CAF	CE	01	00		LDAA	,4F	
3CB2	A6	4F			STAA	1001	Output signal
4	B7	10	01		ANDA	#E0	
7	84	E0			LDAB	54	Check ramp detector alarm
9	D6	54		RAMP			
					BEQ	MLNE	Branch if clear
B	27	02			ADDA	#01	Set alarm #1 bit
D	8B	01			LDAB	55	Check ML detector alarm
F	D6	55		MLNE			
					BEQ		Branch if clear
3CC1	27	02			ADDA	#02	Set alarm #2 bit
3	8B	02			STAA	1008	Display front panel
5	B7	10	08		ANDA	#03	Clear signal bits
8	84	03			LDAB	#01	B = 01
A	C6	01			BITB	,56	Check for 100 m.s.
C	E5	56			BEQ	WDT	
E	27	02			ADDA	#80	Set watch dog timer
3CD0	8B	80			STAA	1005	Output 100 m.s. signal
2	B7	10	05	WDT			
					LDAA	,30	Load meter on Flag
5	A6	30			STAA	1004	Output to meter sign
7	B7	10	04		RTS		
A	39						

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Signal Service

ADDRESS	OPER CODE	OPERAND		LABEL	MNEM.		COMMENTS
3CDB	CE	01	00		LDX	#0100	IR = 0100
E	86	01			LDAA	#01	
3CE0	A4	30			ANDA	,30	Meter on flag set?
2	26	24			BNE	CYTM	
4	86	80			LDAA	#80	
6	A7	4F			STAA	,4F	Set signal green
8	6D	3C			TST	,3C	Off timer expired?
A	27	03			BEQ	START	
C	6A	3C			DEC	,3C	Off timer -1
E	39				RTS		
F	6D	31		START	TST	,31	Start meter flag set
3CF1	27	FB			BEQ	RTS	
3	86	01			LDAA	#01	
5	A7	30			STAA	,30	Set meter on flag
7	A6	33			LDAA	,33	
9	A7	34			STAA	,34	Set 1st amber timer
B	6F	31			CLR	,31	Clear start meter flag
D	6F	37			CLR	,37	Cycle timer = 0
F	A6	39			LDAA	,39	
3D01	A7	3A			STAA	,3A	Load min on timer
3	86	40			LDAA	#40	
5	A7	4F			STAA	,4F	Set signal amber
7	39				RTS		
8	A6	38		CYTM	LDAA	,38	A = Cycle time
A	A1	37			CMPA	,37	Cycle timer = 0?
C	26	06			BNE	06	
E	6C	3D			INC	,3D	Set cycle ready Flag
3D10	6F	37			CLR	,37	Cycle timer = 0
2	20	02			BRA	RED	
4	6C	37			INC	,37	Cycle timer + 1
6	86	20		RED	LDAA	#20	
8	A4	4F			ANDA	,4F	Signal red?
A	27	3B			BEQ	GRN	
C	A6	36			LDAA	,36	Min red expired?
E	27	03			BEQ	03	
3D20	6A	36			DEC	,36	Min red timer -1
2	39				RTS		
3	6D	3E			TST	,3E	Stop meter flag Set?
5	27	11			BEQ	READY	
7	6D	3A			TST	,3A	Min on timer = 0
9	26	0D			BNE	READY	
B	86	80			LDAA	#80	
D	A7	4F			STAA	,4F	Set signal green
F	6F	30			CLR	,30	Clear meter on flag

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Signal Service (Cont'd)

ADDRESS	OPER CODE	OPERAND	LABEL	MNEM.		COMMENTS
3D31	6F	3E		CLR	,3E	Clear stop meter flag
3	A6	3B		LDAA	,3B	
5	A7	3C		STAA	,3C	Load Min off timer
7	39			RTS		
8	6D	3D	READY	TST	,3D	Cycle ready flag set?
A	26	01		BNE		
C	39			RTS		
D	A6	3F		LDAA	,3F	Load max green time
F	A7	40		STAA	,40	
3D41	A6	41		LDAA	,41	Load Min green time
3	A7	42		STAA	,42	
5	6D	43		TST	,43	Demand flag set?
7	26	01		BNE		
9	39			RTS		
A	6F	3D		CLR	,3D	Clear cycle ready flag
C	86	80		LDAA	#80	
E	A7	4F		STAA	,4F	Set signal green
3D50	6D	3A		TST	,3A	Min on timer = 0
2	27	02		BEQ		
4	6A	3A		DEC	,3A	Min on timer -1
6	39			RTS		
7	86	80	GRN	LDAA	#80	
9	A4	4F		ANDA	,4F	Signal green?
B	27	28		BEQ	AMB	
D	6D	42		TST	,42	Min green expired?
F	27	03		BEQ	MAXG	
3D61	6A	42		DEC	,42	Min green -1
3	39			RTS		
4	6D	40	MAXG	TST	,40	Max green expired?
6	27	07		BEQ	AMT	
8	6A	40		DEC	,40	Max green -1
A	6D	44		TST	,44	Passage tetector set?
C	26	01		BNE	AMT	
3	39			RTS		
F	6D	47	AMT	TST	,47	Amber option?

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Signal Service (Cont'd)

ADDRESS	OPER CODE	OPERAND	LABEL	MNEM.		COMMENTS
				BNE	AMOP	
3D71	26	09		LDAA	,35	
3	A6	35		STAA	,36	Load min red timer
5	A7	36				
				LDAA	#20	
7	86	20		STAA	,4F	Set signal red
9	A7	4F		RTS		
B	39					
C	A6	48	AMOP	LDAA	,48	
E	A7	34		STAA	,34	Load amber timer
3D80	86	40		LDAA	#40	
2	A7	4F		STAA	,4F	Set signal amber
4	39			RTS		
5	86	40	AMB	LDAA	#40	
7	A4	4F		ANDA	,4F	Signal amber?
9	26	01		BNE		
B	39			RTS		
C	6D	34		TST	,34	If yes, amber timer = 0?
				BEQ		
E	27	03		DEC	,34	Amber timer -1
3D90	6A	34		RTS		
2	39					
3	A6	35		LDAA	,35	
5	A7	36		STAA	,36	Load min red timer
				LDAA	#20	
7	86	20		STAA	,4F	Set signal red
9	A7	4F		RTS		
B	39					

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Detector Checks

ADDRESS	OPER CODE	OPERAND		LABEL	MNEM.		COMMENTS
3B3A	C6	01			LDAB	#01	Set detector pointer
C	CE	00	90		LDX	0090	IR = Vehi ctr address
F	86	05			LDAA	#05	Lane ctr = 5
3B41	97	02			STAA	02	
3	A6	01		LOAD	LDAA	,01	A = Vehi counts
5	81	02			CMPA	#02	A = A-2
7	2D	0A			BLT	BAD	Bad if result <0
9	6F	02			CLR	,02	Clear check counter
B	53				COMB		B = $\bar{B}$
C	D4	55			ANDB	55	Clear alarm bit
E	D7	55			STAB	55	
3B50	53				COMB		B = $\bar{B}$
1	20	1A			BRA	Lane	Next lane
3	6C	02		BAD	INC	,02	Check ctr + 1
5	86	05			LDAA	#05	
7	A1	02			CMPA	,02	A = 5-check ctr
9	2D	12			BLT	Lane	Next lane
B	86	06			LDAA	#06	
D	B1	01	5B		CMPA	015B	Past 6 AM ?
3B60	2E	09			BGT	Lane	No, to next lane
2	86	01			LDAA	#01	
4	B4	01	5F		ANDA	015F	Sunday?
7	26	04			BNE	Lane	Yea, next lane
9	DA	55			ORAB	55	
B	D7	55			STAB	55	Set detector alarm
D	58			LANE	ASLB		Shift lane pointer
E	08				INX		IR = IR+1
F	08				INX		IR = IR+1
3B70	08				INX		IR = IR+1
1	7A	00	02		DEC	0002	Lane counter -1
4	26	CD			BNE	LOAD	
6	96	B2		RAMP	LDAA	B2	A = demand Veh counts
8	90	B5			SUBA	B5	(dem cts)-(Pass cts)
A	2B	10			BMI	DEMA	Check demand detr
C	81	02			CMPA	#02	Difference -2
E	2D	06			BLT	CLRP	Clear if less than 2
3B80	86	02			LDAA	#02	Set passage detector alarm
2	97	54			STAA	54	
4	20	0F			BRA	Used	

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Detector Checks
(Cont'd)

ADDRESS	OPER CODE	OPERAND		LABEL	MNEM.		COMMENTS
6	86	FC		CLRP	LDAA	#FC	Clear ramp detr alarm
8	94	54			ANDA	54	
A	97	54			STAA	54	Restore alarm byte
C	39				RTS		
D	40			DEMA	NEGA		Reset (-) bit
E	81	02			CMPA	#02	A-2
3B90	2D	F4			BLT	CLRP	Clear ramp detr alarm
2	7C	01	54		INC	0154	Set demand detr alarm
5	96	50		USED	LDAA	50	A = ramp detector used
7	94	54			ANDA	54	Clear unused alarm
9	97	54			STAA	54	Restore alarm bits
B	96	51			LDAA	51	A = ML detector used
D	94	55			ANDA	55	Clear unused alarm
F	97	55			STAA	55	Restore alarm bits
3BA1	39				RTS		

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CONSOLE SERVICE

ADDR	OPER	OPERAND		LABEL	MNOMONIC		COMMENTS
3D9C	B6	10	04		LDAA	1004	Is display switch on?
F	84	10			ANDA	#10	
3DA1	26	01			BNE	START	Yes
3	39				RTS		No
4	CE	01	00	START	LDX	0100	I.R. = 0100
7	B6	10	0A		LDAA	100A	Input display select switch
A	44				LSRA		
B	44				LSRA		
C	44				LSRA		
D	44				LSRA		
E	81	03			CMPA	#03	sw = 03, display memory
3DB0	23	7C			BLS	CON	
2	81	04			CMPA	#04	sw = 04, display time-of-day
4	27	05			BEQ	05	
6	81	05			CMPA	#05	sw = 05, display Julian day
8	27	3D			BEQ	3D	
A	39			RTN	RTS		
B	B6	10	04	TIME	LDAA	1004	Check load switch position
E	84	20			ANDA	#20	
3DC0	27	21			BEQ	21	
2	B6	10	08		LDAA	1008	If set, load Input Data(MSB)
5	A7	5B			STAA	,5B	
7	B6	10	07		LDAA	1007	Load Input Data (LSB)
A	A7	5A			STAA	,5A	
C	B6	10	05		LDAA	1005	Load spare switches
F	A7	57			STAA	,57	
3DD1	B6	10	04		LDAA	1004	Load manual rate
4	84	0F			ANDA	#0F	
6	A7	5C			STAA	,5C	
8	5F				CLRB		B = 0
9	0D				SEC		
A	59			PLLO	ROLB		B = 01
B	4A				DECA		A = A-1
C	26	FC			BNE	PLLO	
E	E7	5F			STAB	,5F	
3DE0	7F	10	00		CLR	1000	
3	C6	20		TMOT	LDAB	#20	B = 20
5	A6	5C			LDAA	,5C	
7	8D	2A			BSR	OUT2	Display manual rate
9	A6	5B			LDAA	,5B	
B	8D	26			BSR	26	
D	A6	5A			LDAA	,5A	Display input data
F	8D	22			BSR	22	

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ADDR	OPER	OPERAND		LABEL	MNOMONIC		COMMENTS
3DF1	A6	57			LDAA	,57	Display spare switches on spare lites
3	B7	10	03		STAA	1003	
6	39			RTN1			
7	C6	08		JDAY	LDAB	#08	B = 08
9	A6	5E			LDAA	,5E	
B	8D	16			BSR	16	Display Julian day (MSB)
D	A6	5D			LDAA	,5D	
F	8D	12			BSR	12	Display Julian day (LSB)
3E01	B6	10	04		LDAA	1004	
4	84	20			ANDA	#20	Check load switch
6	27	0B			BEQ		
8	B6	10	03		LDAA	1008	Update Julian calender
B	A7	5E			STAA	,5E	
3E0D	B6	10	07		LDAA	1007	
0	A7	5D			STAA	,5D	
2	39			RTN2	RTS		
3	F7	10	07	OUT2	STAB	1007	Strobe hex display
6	36				PSHA		Stack = A
7	44				LSRA		
8	44				LSRA		
9	44				LSRA		
A	44				LSRA		
B	8B	70			ADDA	#70	
D	B7	10	06		STAA	1006	Blank displays
3E20	32				PULA		
1	54				LSRB		
2	F7	10	07		STAB	1007	Strobe next display
5	84	0F			ANDA	#0F	
7	8B	70			ADDA	#70	
9	B7	10	06		STAA	1006	Display content
C	54				LSRB		
D	39				RTS		
E	B6	10	0A	CON	LDAA	100A	Input memory address
3E31	A7	0E			STAA	,0E	
3	B6	10	09		LDAA	1009	
6	A7	0F			STAA	,0F	
8	EE	0E			LDX	0E	I.R. = memory address
A	B6	10	04		LDAA	1004	
D	84	20			ANDA	#20	Check load switch
F	27	05			BEQ	05	
3E41	B6	10	07		LDAA	1007	Enter new data into memory
4	A7	00			STAA	,00	
6	C6	02		DISM	LDAB	#02	B = 02
8	A6	00			LDAA	,00	A = memory address
A	36				PSHA		A = stack
B	44				LSRA		
C	44				LSRA		
D	44				LSRA		

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CONSOLE SERVICE

ADDR	OPER	OPERAND		LABEL	MNOMONIC		COMMENTS
3	44				LSRA		
F	8B	40			ADDA	#40	A = A+40
3E51	8D	07			BSR	07	Branch to display
3	32				PULA		
4	84	0F			ANDA	#0F	
3E56	8B	40			ADDA	#40	
8	C6	01			LDAB	#01	
A	F7	10	07	OUT	STAB	1007	Strobe hex display
D	B7	10	06		STAA	1006	Display memory content
3E60	39				RTS		

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VII. APPENDIX

Type 140 Controller Specifications

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INTRODUCTION

The Type 140 controller system, as described in these specifications, will be used as a freeway on-ramp access controller. These specifications are primarily microprocessor hardware specifications. All applications software for the programmable controller will be developed by the Department of Transportation.

Some Type 140 controller systems will be used as part of interconnected freeway control systems. Some, with other software, will stand alone as a local traffic sensitive controller. Other software will enable it to act as versatile "time-of-day" controller that changes control modes or rates many times during peak traffic period with a schedule based on historical data.

The basic hardware specified for the Type 140 controller system with software variations will be capable of any one and many combinations of the functions as follows:

1. Actuate Signals and Signs

   The microprocessor controller unit will handle all signal phase timing. Latched output bits will drive AC load switches to actuate traffic signal heads, extinquishable message signs or other devices that may be located on the on-ramp or on the nearby city street.

2. Collect Occupancy and Count Data From Vehicle Detectors

   Vehicle detectors will be located in each main freeway lane and at several locations along each on-ramp. The controller will scan each detector 20 times per second. The controller will store occupancy and vehicle count data for the most recent 3 to 5 minutes.

3. Transmit Data and Receive Instructions From Master Terminal

   The controller will be programed to transmit through its modem any of its data base or any data stored elsewhere in Random Access Memory upon request from a minicomputer acting as its master terminal. The controller will likewise accept instructions from the master to change timing data, threshold numbers or anything else stored in Random Access Memory. Some data will be transmitted regularly as often as each 6 or 10 seconds. Other data may be requested by the master as infrequently as once a month.

4. Operate as a Slave of a Master with Backup Program When Communications Fail

   The controller will be programmed to use the metering rates selected by a master. It will be programmed to recognize

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communication failures and to make its own decisions using "time-of-day" programs or local traffic data--or some combination of the two methods.

5. Operate as a Stand Alone "Time-of-Day" Controller

Some controllers will be programed to select metering rates at specific times on a 7-day clock. They will have the capacity to store 100 times to the nearest minute. They will store the appropriate function to be implemented with each stored time. Most "time-of-day" controllers will transmit data to a master. These data will be used to establish and update historical traffic demands. Some of these controllers will accept real time override instructions from the master.

6. Operate as a Stand Alone Traffic Sensitive Controller

Some controllers will be programed to select metering rates using variable threshold levels compared to data in its own occupancy and count data base. In some cases these controllers will also maintain a "time-of-day" control schedule that will override the traffic sensitive logic. In some cases the "time-of-day" schedule will be a secondary fall-back routine in the event of critical detector failure.

7. Monitor Vehicle Detectors

For many years we have found it very difficult to maintain accurate and consistant vehicle detection. The expected detector failure frequency makes it unthinkable to use detector data for freeway control without knowing when the detector is not working properly. The Type 140 controller unit will be programmed to recognize from input data that detectors have failed-on, failed-off, or do not compare as they should with other detectors in the system. The controller will be programmed to identify the failure and select the best available fall-back operating mode until help arrives.

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Section I

Contract Requirements

The equipment to be furnished shall consist of the following quantities.

Quantity	Item
200 Ea	Type 140 Controller Cabinet
2000 Ea	Detector Amplifier Module
150 Ea	Modem
4 Ea	Master Communication Terminal
210 Ea	Type 140 Controller Unit
45 Ea	Control Console
5 Ea	Programming Systems

All equipment furnished for this order shall be new.

A supplier bidding on any one of the following subgroups of items must bid on all of the items in the particular subgroup or his bid will be considered invalid.

Subgroup I - Type-140 Controller cabinet

Subgroup II - Detector amplifier module

Subgroup III- Modem, Master Communication Terminal, Type-140 Controller Unit, Control Console and Programming Systems.

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Quantity	Item	Delivery For Testing (In Calendar Days From P.O. Date)	Maximum Time for Delivery and Inspection (In Calendar Days From Date of P.O.)
SHIPMENT A		90 Days	100 Days
10 Ea	Detector Amplifier Module		
1 Ea	Type 140 Controller Unit		
1 Ea	Control Console		
1 Ea	Programming System		
SHIPMENT B		150 Days	171 Days
40 Ea	Type 140 Controller Cabinet		
390 Ea	Detector Amplifier Module		
30 Ea	Modem		
3 Ea	Master Communication Terminal		
40 Ea	Type 140 Controller Unit		
9 Ea	Control Console		
4 Ea	Programming System		
SHIPMENT C		180 Days	201 Days
40 Ea	Type 140 Controller Cabinet		
400 Ea	Detector Amplifier Module		
30 Ea	Modem		
45 Ea	Type 140 Controller Unit		
9 Ea	Control Console		
SHIPMENT D		210 Days	231 Days
40 Ea	Type 140 Controller Cabinet		
400 Ea	Detector Amplifier Module		
30 Ea	Modem		
44 Ea	Type 140 Controller Unit		
8 Ea	Control Console		
SHIPMENT E		240 Days	261 Days
40 Ea	Type 140 Controller Cabinet		
400 Ea	Detector Amplifier Module		
30 Ea	Modem		
40 Ea	Type 140 Controller Unit		
9 Ea	Control Console		

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Quantity	Item	Delivery For Testing (In Calendar Days From P.O. Date)	Maximum Time for Delivery and Inspection (In Calendar Days From Date of P.O.)
SHIPMENT F		270 Days	291 Days
40 Ea	Type 140 Controller Cabinet		
400 Ea	Detector Amplifier Module		
30 Ea	Modem		
40 Ea	Type 140 Controller Unit		
9 Ea	Control Console		

Within the specified number of calendar days from the awarding of the purchase order, each complete shipment described above shall be delivered to the California Department of Transportation, Service and Supply, 5990 Folsom Boulevard, Sacramento, CA 95819. Each shipment shall be complete prior to delivery for acceptance testing. Delivery for acceptance testing of any shipment shall not be made until the previous shipment has been accepted.

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Change orders amending, modifying or terminating the contract, including any modification of the compensation payable, may be issued only by the State Procurement Office. All such change orders shall be in writing and shall be issued only upon the written request of the requisitioning agency with the written concurrence of the Contractor. Termination, as that term is used in this section, does not include termination for default of the Contractor.

BID ATTACHMENTS

Each bidder shall furnish with his bid one reference manual for the microprocessor proposed. The Department of Transportation will review each of the bidder's submissions. The Department of Transportation's review shall not relieve the successful bidder of his full responsibility for meeting all specifications.

PERFORMANCE BOND

A performance bond will be required before contract acceptance. The performance bond shall be at least ten percent of the total amount bid for the firm quantities.

PAYMENT

Upon successful completion of the acceptance tests, payment representing ninety-five (95) percent of the bid price for the items included in a shipment will be made to the contractor for the specific shipment. The remaining five (5) percent will be paid to the vendor in one lump sum after all items included in the purchased order have been accepted.

WARRANTY

A six-month warranty, including material, labor, and shipping charges, will be required for all items. The warranty shall begin upon first operation of the item in the respective Department of Transportation District. In no case will the warranty period exceed 12 months after the date of acceptance.

All items returned to the Contractor for warranty repair shall be repaired and returned to the Department of Transportation within two weeks after receipt at the designated repair facility. If the items are not returned within two weeks, a tested loaner shall be provided at no cost to the state until the required original item is returned. Failure to comply with warranty requirements shall be sufficient grounds to prohibit the contractor from bidding on future State of California contracts.

LIQUIDATED DAMAGES

It is agreed by the parties to the contract that in case all the work called for under the contract, in all parts and requirements, is not finished or completed within the contract time set forth

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in the bid unless delay is authorized in writing by the State Procurement Officer, damage will be sustained by the State of California, and that it is and will be impracticable and extremely difficult to ascertain and determine the actual damage which the State will sustain in the event of and by reason of such delay; and it is therefore agreed that the Contractor will pay the State of California an amount as shown in the schedule below, per day for each day's delay in finishing the work beyond the time prescribed, provided the total damages assessed against the Contractor shall in no case exceed 50 percent (50%) of the total value of the entire order; and the Contractor agrees to pay said liquidated damages as herein provided, and in case the same are not paid, agrees that the State may deduct the amount thereof from any money due or that may become due the Contractor under the contract.

Liquidated Damages Schedule

Type 140 Controller Unit	$ 10 per unit per day
Detector Amplifier Module	1 per unit per day
Modem	5 per unit per day
Master Communication Terminal	10 per unit per day
Type 140 Controller Cabinet	10 per unit per day
Control Console	10 per unit per day
Programming System	50 per unit per day

No extension of time will be granted for a delay caused by a shortage of materials.

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CALIFORNIA DEPARTMENT OF TRANSPORTATION

On July 1, 1973, the Department of Transportation succeeded to and was vested with all of the duties, powers, purposes, responsibilities and jurisdiction of the Department of Public Works. Effective on July 1, 1973, all references in the contract documents to Department or Department of Public Works or Director or Director of Public Works shall be deemed to mean the Department of Transportation or the Director of Transportation, respectively, and references to District Engineer shall be deemed to mean District Director of Transportation.

On November 1, 1974, the Department of Transportation was reorganized. The Chief Engineer, Department of Transportation succeeded to and was vested with all the duties, powers, purposes and responsibilities and jurisdiction with regard to construction or maintenance contracts of the State Highway Engineer, Division of Highways. Effective on November 1, 1974, all references in the contract documents to the Engineer or State Highway Engineer shall be deemed to mean the Chief Engineer, Department of Transportation and all references to the Division of Highways in the contract documents shall be deemed to mean the Department of Transportation.

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Section II
Type 140 Controller Cabinet

GENERAL

The Type 140 Controller Cabinet shall comply with the following specifications and attached plan sheets SES-34B and 35A. Further reference in these specifications to the "Plans" shall refer to these sheets. The cabinet shall be furnished and wired complete with all equipment specified, including the following:

- 1 - Detector Rack
- 1 - Police Panel (with "lights" and "police control" switches)
- 1 - Power Distribution Panel (with main circuit breaker, equipment circuit breaker, equipment receptables on front and back, three switching device sockets, and one transfer relay socket)
- 1 - Power Supply
- 1 - Power Supply/MODEM Housing
- 2 - Switching Devices
- 1 - Transfer Relay
- 1 - Watchdog Timer
- 1 - Visual Alarm Light

All fuses, breakers, switches, and indicators, including those on the police panel, shall be readily visible and accessible when the appropriate door is open.

All of the above listed equipment shall be readily removable using common hand tools.

All equipment furnished in the cabinet shall be clearly and permanently labeled. Marker strips on the vehicle detector rack, and the power distribution panel shall be located immediately below the subject module. The strips shall be made of material that can be legibly written on with pencil or ball point pen.

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INTERCHANGEABILITY

It shall be possible to electrically and mechanically interchange any of the following devices with the corresponding device in the California Standard Type 200 Controller Cabinet, a sample of which is located at:

Transportation Laboratory
5900 Folsom Boulevard
Sacramento, California

The devices shall include the following:

Transfer Relay
Detector Rack
Switching Devices

CIRCUIT BREAKER

Circuit breakers shall be approved and listed by UL. The trip and frame size shall be plainly marked. All circuit breakers shall be quick-make, quick-break on either manual or automatic operation. Contacts shall be silver alloy enclosed in an arc quenching chamber. Overload tripping shall not be influenced by an ambient temperature range of from -18°C to 70°C. Minimum interrupting capacity shall be 5,000 amperes, RMS.

CONDUCTORS

Conductors in the controller cabinet between the service terminals and the signal bus and green bus circuit breakers, including the signal common, shall be No. 12 AWG or larger. All other conductors in the line voltage circuits shall be No. 14 AWG, minimum except circuits carrying less than 0.25-ampere.

All conductors not part of a jacketed cable, used in controller cabinet wiring, shall be No. 22 AWG or larger, with a minimum of 19 strands. Conductors shall conform to Military Specifications MIL-W 16878D, Type B or D, Vinyl-Nylon Jacket or irradiated cross-linked polynivylchloride, 600-volt, 105°C, except that, at the contractor's option, conductors No. 14 AWG and larger may be UL Type THHN, 600-volt.

The loop detector lead-in, from the field terminals in the cabinet to the sensor unit, shall be a shielded twisted pair of No. 22 AWG, or larger, conductors.

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All conductors, except those which can be readily traced, shall be labeled. Labels attached to the end of a conductor shall identify the destination of the other end of the conductor.

All conductors used in controller cabinet wiring shall conform to the following color-code requirements:

(A) The grounded conductor of an AC circuit shall be identified by a continuous white or natural gray color.

(B) The equipment grounding conductor shall be identified by a continuous green color or a continuous white color with one or more green stripes.

(C) The ungrounded conductors shall be identified by any solid color not specified in (A) or (B) above.

CONNECTORS

All connectors shall be keyed to prevent accidental insertion of the wrong connector or printed card.

Printed card edge connectors shall have bifurcated, beryllium copper gold-plated contacts.

All pin and socket connectors furnished with the cabinet shall utilize the same contact insertion tool, contact extraction tool, and contact crimping tool.

Connector C2P shall intermate respectively with connector C2S mounted on the controller unit chassis.

Blocks for all pin and socket connectors shall be constructed of diallyl phthalate or better material. Contacts shall be secured in the blocks with springs of stainless steel.

Protection from accidental bending shall be provided for pin contacts.

All cable connectors shall have cable hoods or shields and strain relief clamps.

Pin and socket contacts shall be beryllium copper construction sub-plated with 0.00005-inch nickel and plated with 0.00003-inch gold. Pin diameter shall be 0.062-inch.

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Connector C1P shall contain 104 pin contacts, shall have a "T" handle center fastener, and shall intermate with the C1S connector shown on the Plans and with the C1S connector on the California Standard Type 200 Controller Unit.

Corner guide pins for connector C1P shall be stainless steel and shall be 1.097 inches in length. Corner guide socket assemblies shall be stainless steel and shall be 0.625-inch in length.

DETECTOR RACK

Each detector rack shall utilize 5.25 inch of rack-mounting height. The detector rack shall be capable of housing 14 detector modules described elsewhere in these specifications.

The detector rack shall provide card guides (top and bottom) and a 22-pin edge-connector centered vertically for each detector. The detector rack shall allow air circulation through the top, bottom, and rear of the detector rack.

Four pins (4, 5, 8, 9) on each detector module edge connector shall be wired to four field terminals to provide for two loop detector channels or one magnetometer channel.

Loop 1 and 2 output collectors and emitters (pins 6, 7, 19 and 20) for each slot shall terminate on a terminal block mounted on the rear of the detector rack and shall connect to the proper controller unit inputs in the connector C1S wiring harness.

The detector rack shall be wired as shown on the Plans.

EQUIPMENT LIST AND DRAWINGS

Detailed equipment layout scale drawings and wiring diagrams of all equipment installed in the controller cabinet shall be submitted to the State for approval prior to production.

Cabinet wiring diagrams shall be contained in a heavy duty clear plastic envelope mounted on the inside of the front door.

The contractor shall furnish three sets of controller cabinet schematic wiring diagrams. With each controller cabinet, the contractor shall furnish one copy of a schematic diagram and one copy of a layout diagram including component location and identification for each P.C. board within the controller cabinet. Component identification shall include manufacturer's name and part number. The diagrams shall be non-proprietary and shall identify all circuits and components in such a manner as to be

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readily interpreted. Three sets of circuit diagrams of the plug-in modules shall also be furnished. The wiring and circuit diagrams shall be submitted with each controller when it is delivered for testing.

All conductor labeling on the schematic wiring diagrams shall be identical with the labeling actually on the conductors.

HOUSING

The Type 140 controller cabinet shall be a raintight steel cabinet with dimensions as shown on the Plans. The cabinet shall have a factory applied rust resistant prime coat and the exterior shall be finished with a baked enamel coat conforming to Federal Standard 595a, Color No. 34672. The basic cabinet and door shall be 14 gauge minimum thickness steel, with all seams continuously welded. The housing shall have single doors, front and rear, each equipped with a keyed tumbler lock. Locks shall be compatible with existing State of California Controller Cabinet keys. Two keys shall be provided per cabinet. When the doors are closed and latched with key removed, the doors shall lock. The latching handles shall have provisions for padlocking in the latched position. Details of construction may vary from that shown on the Plans if approved by the State. The front door shall have a continuous hinge near the left edge when viewed from the front. The rear door shall have a continuous hinge mounted near the right edge when viewed from the rear. Front and rear doors shall be provided with catches to hold the door open at 90° and 180° $\pm$ 10°. The catches shall securely hold the door open until released.

The police panel door shall be equipped with a lock for a master keyed police key. The police panel shall be mounted on the side of the Type 140 controller cabinet as shown on the Plans. Two keys shall be furnished with each cabinet for the police lock. Each police key shall have a shaft at least 1-3/4 inch in length.

The cabinet base layout shall accommodate the anchor bolts and conduits as shown on the Plans.

Each controller cabinet shall be provided with louvered vents in the front door with a permanent metal filter, which will permit the fan to pass the volume of air specified. The louvered vents shall be designed and constructed such that a horizontal stream of water from a pressure head such as a rain-bird sprinkler or other type sprinkler will not enter the cabinet.

Each controller cabinet shall be equipped with an electric fan with ball or roller bearings and a capacity not less than 100 cubic feet per minute.

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The fan shall be mounted in a raintight housing attached to the top of the controller cabinet as shown on the Plans.

The fan shall be thermostatically controlled and shall be manually adjustable to turn on at between 90°F and 150°F with a differential of not more than 10°F between automatic turn on and turn off. The cabinet fan circuit shall be fused at 125 percent of the ampacity of the fan motor installed.

A standard EIA 19-inch rack shall be inside the cabinet for mounting the Type 140 controller unit, the detector rack, power supply/MODEM housing, and the power distribution panel. The rack shall consist of front rails drilled and tapped (10-32) with EIA spacing. The mounting face of the rear rails shall be 23 inches behind the front rails. Chassis supporting angles extending between the front and rear rails shall be supplied to distribute and support the weight of the controller unit. Each angle shall be 21 inches deep and 3 inches wide.

The inside walls, doors, and ceiling of the housing shall be insulated with the equivalent of 1/2-inch thick, fire retardant material with a K-factor of 0.25.

The housing shall include lifting eyes to be used when placing the cabinet on the foundation.

Two "L" hook holders shall be provided on the back of the front door as shown on the Plans for control console mounting.

POLICE PANEL

A police panel shall be provided behind the police panel door and shall contain a DPST toggle switch labeled "LIGHTS", "ON-OFF" and a SPST switch labeled "POLICE CONTROL", "ON-OFF". The switches shall have contacts rated for 20 amperes at 125 volts AC. The switches shall be wired as shown on the Plans.

POWER SUPPLY

A power supply shall be provided in the cabinet to operate all peripheral hardware installed in the cabinet. The peripheral hardware shall include all electrical equipment not wholly dependent on line voltage power.

The power supply shall be housed in the 19-inch rack location shown on the Plans.

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The power supply shall have a minimum output capacity of 5 amperes at 24 volts. The power supply output shall be maintained throughout line power interruptions of 17 ms and less. All DC power shall have line and load regulations better than 1 percent and ripple of less than 5 millivolts.

All outputs shall be short-circuit protected. The power supply front panel shall include:

All fuses or circuit breakers
Pilot lamp
Test points or meter for monitoring output

POWER SUPPLY/MODEM HOUSING

The power supply/MODEM housing shall include a rack shelf and front panel.

The 19-inch wide steel shelf shall be mounted in the EIA rack with the depth of the shelf such as to support the power supply and MODEM units. The shelf shall be perforated to allow ventilation.

A front panel shall be provided for the power supply/MODEM cavity. The blank panel shall have a continuous hinge on the left side and a spring catch and pull knob that protrudes no more than 1/2-inch.

Attaching the power supply to the front panel such that the panel and power supply are held in place as a unit by captive wing screws is an acceptable alternative mounting.

POWER DISTRIBUTION PANEL

The power distribution panel shall be furnished and mounted on the EIA 19-inch rack utilizing 7 inches of rack height. All equipment shall be readily accessible for ease of replacement.

The following equipment shall be provided with the panel:

1 - Power line surge protector

1 - Equipment circuit breaker

2 - Equipment receptacles (one on front panel and another on back accessed from back door)

1 - Main circuit breaker

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3 - Switching device sockets

1 - Transfer relay socket

The load switching device sockets shall mate with and support a California Standard Solid State Switching Device as described elsewhere in these specifications.

The equipment circuit breaker shall be single pole, automatic trip, rated 15 amperes at 125 volts AC.

The main circuit breaker shall be the same as the equipment breaker except rated for 30 amperes.

Equipment receptacles shall be NEMA 5-15R duplex type.

The equipment receptacles shall have ground fault circuit interruption as defined in the National Electrical Code. Circuit interruption shall occur between 4 and 6 milliamperes of ground fault current.

WATCHDOG TIMER

A watchdog timer shall be furnished and wired into the cabinet as shown on the Plans. The watchdog timer output from the Type 140 controller unit will change state every 100 milliseconds under program control. Failure to receive this change of state for one second shall cause the watchdog timer to output an open circuit. A switch shall be provided with the watchdog timer to inhibit its operations.

The watchdog timer output shall be a relay with contacts rated for 120 volt operation.

PRINTED BOARDS

All printed circuit boards shall be as described in Type 140 Controller Unit Section of these specifications.

SWITCHING DEVICES

Traffic signal lamp circuits and visual alarm light shall be controlled by switching devices.

Each switching device shall control three lamp circuits by using solid state load switches. Each load switch shall have a minimum rating of 8 amperes at 120 volts AC, for tungsten lamp or gas tubing transformer circuit.

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Indicators for each lamp circuit output shall be visible when viewing the installed switching device.

Solid state load switches shall employ no moving parts in the output circuit to the signal lamps.

The load switch shall utilize zero-point switching, with turn-on at the zero voltage point and turn-off at the zero current point of the power line sunusoid ± 5 degrees.

The input command signal shall be the equivalent of an open collector, NPN transistor as provided under Type 140 Controller Unit.

A low-level input signal (saturated NPN transistor, 0 to +2.0 volts, DC) shall cause the switching device to be energized. A high-level input signal (cut-off NPN transistor) shall cause the switching device to be de-energized.

During normal operation (no circuit or one circuit energized) the switching device shall not use more than 20 milliamperes from a +24 volt DC source.

The load switch shall not apply more than 30 volts, peak, to the signal input line, nor shall the input signal source be required to sink more than 10 milliamperes.

Construction of the switching device shall be such that personnel inserting or removing the module will not be exposed to live parts and will not be required to insert their hands or fingers into the load rack. Hand pulls shall be provided.

SURGE ARRESTOR

A surge arrestor shall be furnished to reduce the effects of voltage transients on each power line and shall have minimum ratings as follows:

Recurrent peak voltage	184 volts
Energy rating, maximum	20 joules
Power dissipation, average	0.85 watt
Peak current for pulses less than 7 microseconds	1250 amperes

Standby current shall be 1 milliampere or less for 60 Hz sinusiodal input.

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TERMINAL BLOCKS

Terminal blocks shall be provided for terminating field conductors.

The field wire terminal blocks shall be barrier type with marker strip and shall be provided with 10 - 32 minimum, nickel or cadmium plated brass binder head screws and inserts. The terminal blocks shall be readily accessible through the cabinet rear door.

Power line service terminals shall be labeled L1 and N, and shall be covered with a clear insulating material to prevent inadvertent contact.

One or more field terminals shall be provided for each line voltage field circuit. A minimum of 12 unused field terminal positions shall be provided for additional line voltage circuits.

Four field terminals positions shall be provided for each vehicle detector module. Two positions are to be used for loop detector modules. All four positions are to be used when magnetometer detector modules are inserted into the detector rack.

A 16 position barrier type terminal block (TB1) shall be furnished for terminating conductors from connector C2P as indicated on the Plans.

The terminal blocks shall be rated for 20 amperes and 1000 volts, RMS, minimum.

No more than three conductors shall be brought to any one terminal. Two flat metal jumpers, straight or U-shaped, may be placed under a terminal screw. At least two full threads of all terminal screws shall be fully engaged when the screw is tightened. No live parts shall extend beyond the barrier.

Terminals shall be a minimum of 12 inches above the bottom of the cabinet.

TRANSFER RELAY

The transfer relay shall be mounted on the same chassis as the signal switching devices. The relay shall be provided with a dust cover, having no exposed live parts, and shall intermate with a Cinch Jones Socket S-2408-SB connected as shown on the Plans.

The transfer relay shall be used to turn on the alarm light atop the cabinet and disable all switching devices when the police panel "lights" switch is switched to off position or when the watchdog monitor opens the circuit as shown on the Plans.

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The relay shall have double pole double-throw contacts and shall be designed for continuous duty, operating between the ambient temperatures from -18°C to +70°C.

Contact points shall be of fine silver, silver-alloy, or approved alternative material.

Contact points and contact arms shall be capable of carrying a current of 20 amperes per contact at 120 volts, 60 Hz, AC.

The relay shall be rated for continuous duty.

A leakage resistor, which will permit a small amount of current to pass through the relay coil if the contacts should remain closed after the coil circuit is opened, shall be installed with the transfer relay to overcome residual magnetism effects.

Relay shall conform to the requirements of the following tests:

Load Test: Relay shall show no failure while making, carrying and breaking a 30-ampere, 120-volt, AC, traffic signal lamp load through 10,000 cycles at the rate of 10 cycles per minute. The cycle shall be 50 percent on and 50 percent off.

Overload Test: Overload test shall consist of the following: Relay shall be electrically and mechanically operative after a momentary current of 100 amperes, 120 volts, AC is applied to each set of closed contacts at least five times with a minimum of 2 minutes between applications of current.

Relay shall not break down or flashover while carrying a load of 40 amperes, 120 volts for at least 50 cycles at the rate of 5 cycles per minute. Cycle shall be 50 percent on and 50 percent off.

Dielectric Strength Test: Relay shall withstand a potential of 1,500 volts at 60 Hz between insulated parts and between current carrying parts and grounded or non-current carrying parts.

VISUAL ALARM LIGHT

A vandal resistant visual alarm light shall be mounted on the roof of the cabinet as shown on the Plans. The alarm light shall be actuated by one of the switching devices or by a transfer relay as shown on the Plans. The light shall be visible from 360 degrees and shall have a clear polycarbonate lens, 2-1/2 inches in diameter. Lamp shall be 15 watts, 120 volts, AC with medium base.

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WIRING

The cabinet wiring shall conform to the following specifications:

All live parts or conductors which could be a hazard to personnel when either door is open shall be covered with suitable insulating material.

Cabinet circuit wiring shall be arranged to provide safe and reliable operation of the signal heads during normally encountered circumstances (power restart, changing vehicle detector modules, etc.). Care shall be exercised in conductor routing to minimize interference and crosstalk. Workmanship shall be in accordance with the highest industry standards. All cabling shall be sheathed or tied and dressed in the cabinet in an orderly and neat manner to facilitate ease of maintenance.

The cabinet shall be wired to conform with the one-line diagram on the Plans.

The grounded conductor (signal common) terminal bus shall not be grounded to the controller cabinet or connected to logic ground and shall provide a minimum of 10 terminals for connection of field conductors.

An equipment grounding conductor bus shall be provided in each controller cabinet. The bus shall be grounded to the cabinet.

Conductors from connector C1P to the detector rack shall be of sufficient length to connect to any detector output terminal.

Cabling shall be routed to prevent conductors from being in contact with metal edges. Cabling shall be arranged so that any removable subassembly may be removed without disturbing conductors not associated with that subassembly.

One outlet receptacle NEMA Type L5-15R, for Type 140 Controller Unit shall be provided.

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INDUCTIVE LOOP DETECTOR AMPLIFIER MODULE

The inductive loop detector amplifier module shall insert into and connect to the "DETECTOR RACK" described in Section II, and shall be electrically and mechanically interchangeable with the detector module in the California Standard Type 200 Controller. The amplifier shall be mounted on an edge-connected, printed circuit board of the dimensions shown on the plan SES34B. The printed circuit board shall conform to printed circuit board specifications in Section VI. Each amplifier channel shall draw not more than 100 ma at 24 VDC and shall operate with the power supply described in Section II.

The amplifier module front panel shall be provided with a hand pull to facilitate insertion and removal from the Detector Rack.

Each amplifier channel shall have a front panel mounted indicator to provide a visual indication of each vehicle detection. The indicator shall be rated for at least 50,000 hours rated life. The indicator shall have brightness not less than 2.0 milli-candella and shall be visible when viewed in sunlight. Initial tuning may be automatic or manual. Manual tuning operations shall be accomplished by using only front panel controls. The amplifier shall be capable of tuning to loops with inductance in the range 50 to 500 microhenries.

All modules supplied shall be identical. The amplifier output shall be an NPN open collector and shall be compatible with the Controller Unit inputs described elsewhere in these specifications. Each output line shall have blocking diodes installed to prevent the sensor unit from "sourcing" power into the Controller Unit inputs.

MULTI CHANNEL AMPLIFIERS

Modules containing more than one input-output loop detector sensor circuit channel may be furnished. No more than two channels shall be provided for each detector rack slot and no more than two slots shall be occupied by any module.

When modules containing more than one channel are furnished, one additional module for every two controller cabinets must be supplied in lieu of the single channel modules specified.

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SENSITIVITY

Each amplifier module shall have a minimum of two sensitivity settings which are selectable from the front panel. The more sensitive setting (high) shall consistently respond to an inductance change of 0.02 percent. The less sensitive setting (OCC) may be chosen by the manufacturer so that accurate and repeatable occupancy measurements may be obtained. This setting must cause the amplifier to respond to a nominal change in inductance which is in the range .15 percent to .4 percent. All modules must have sensitivities which differ by not more than ± .05 percent change in inductance from the nominal value chosen. The amplifier shall not respond to inductive changes less than .1 percent in the OCC setting.

RESPONSE TIME

Response time of the amplifier module for the OCC setting shall be less than 20 milliseconds. That is, for any negative inductive change which exceeds its sensitivity threshold, the amplifier shall output a ground true logic level within 20 milliseconds. When such change is removed, the output shall become an open circuit within 20 milliseconds. For test purposes, the negative change of inductance will be maintained for a minimum of 100 milliseconds and a maximum of 600 milliseconds after it is applied. When the differences between the length of time, the inductance change is applied, and the corresponding ground true output time are averaged over ten trials, the value of that average difference shall not exceed 10 milliseconds.

The response time of the amplifier module for the HIGH setting shall be less than 250 milliseconds for a 1.0 percent inductance change.

HOLD TIME

The amplifier in the OCC position shall indicate the continuous presence for four minutes minimum of a vehicle causing a change in inductance of 1 percent or greater. The amplifier in the HIGH position shall indicate the continuous presence for three minutes minimum of a vehicle causing a 0.02 percent inductance change.

GENERAL OPERATIONAL REQUIREMENTS

The amplifier shall begin normal operation within five minutes after the application of power.

The amplifier module shall not crosstalk, interfere with, or be sympathetic to operation of any other amplifier module and shall not detect vehicles three feet or more from a single 6' x 6' three-turn loop with 50 feet of lead-in in either sensitivity position.

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The operation of the amplifier shall not be affected by changes in the inductance of the loop caused by environmental changes with the rate of temperature change not exceeding one degree Fahrenheit per three minutes. The opening or closing of the controller cabinet door with a differential temperature of 30°F between the inside and outside shall not affect the proper operation of the amplifier.

The test loop configurations will include one 6' x 6' three-turn loop with 300 feet of lead-in cable with an approximate total inductance (loop plus lead-in) of 140 microhenries and one 6'x 6' three-turn loop with 750 feet of lead-in cable with an approximate total inductance of 220 microhenries and four 6' x 6' three-turn loops in a series-parallel arrangement with 300 feet of lead-in cable and an approximate total inductance of 120 microhenries.

The quality or Q factor of test loops as well as field loops will be greater than or equal to five (5) for loop-amplifier resonant frequencies in the range 20 kilohertz to 90 kilohertz.

If a passenger car remains stationary over a loop for up to 30 minutes, the amplifier shall be restored to full performance within 20 seconds of the car's leaving.

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Section VI
Type 140 Controller Unit

The Type 140 Controller unit shall consist of the following major components:

Chassis
DC Power Supply
Central Processing Unit (CPU)
Memories
Power/Restart
Input/Output Interface
Real Time Clock
Down Time Accumulator
Communications Module

DOCUMENTATION

The contractor shall furnish 1 set of controller unit schematic wiring diagrams and 1 set of PC board layouts with each controller unit.

The diagrams shall identify all circuits and components in such a manner as to be readily interpreted. The wiring and circuit diagrams shall be submitted with each controller unit when it is delivered for testing.

The contractor shall furnish a maintenance manual for the controller units. The maintenance manual and operation manual may be combined into one manual. The maintenance manual or combined maintenance and operation manual shall be submitted at the time the controllers are delivered for testing. 25 copies of the maintenance manual shall be supplied. The maintenance manual, shall include, but need not be limited to, the following items:

(a) Specifications

(b) Design Characteristics

(c) General operation theory

(d) Function of all controls

(e) Trouble shooting procedure (diagnostic routine)

(f) Block circuit diagram

(g) Geographical layout of components

(h) Schematic diagrams

(i) List of replaceable component parts with stock numbers

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CHASSIS

The Type 140 Controller unit shall be housed in a metal enclosure not more than 10½" high and 20" deep, and mountable in a 19" rack. The enclosure shall be designed for convenient removal of printed circuit boards without the use of tools. Fuses and connectors shall be readily accessible and shall be replaceable without the use of tools. Ventilation shall be provided where necessary.

FRONT PANEL

The front panel of the Type 140 Controller unit shall be as shown on the plans. It shall be securely fastened to the chassis and removable with common hand tools. It shall be electrically connected to the controller unit by means of a connector or a barrier type terminal strip. The indicator lights and switches shall be the same types as those used on the control console.

PIN CONNECTORS

Blocks for all connectors shall be constructed of diallyl phthalate or an approved alternate material. Contacts shall be secured in the blocks with springs of stainless steel.

Contacts shall be beryllium copper construction, subplated with 0.00005-inch nickel and plated with 0.00003-inch gold. Sockets shall accept pin contacts 0.062-inch in diameter. The lead-in connector shall contain the socket contacts.

Corner guide pin assemblies for pin connectors shall be stainless steel and shall be 1.097 inches in length. Corner guide socket assemblies shall be stainless steel and shall be 0.625 inch in length.

A 104 socket connector (C2S) shall be securely fastened to the left front of the chassis. This connector shall protrude a maximum of ½" through a hole in the front panel.

A 104 socket connector (C1S) shall be mounted on the rear panel of the chassis. This connector shall not protrude more than 3/4" from the rear panel. The connectors shall be wired with the functions shown on the plans.

PRINTED CIRCUIT BOARD CONNECTORS

All P.C. board connectors shall be keyed to prevent accidental insertion of the wrong connector or printed circuit card.

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Printed circuit card edge connectors shall have bifurcated, beryllium copper, gold-plated contacts.

PRINTED CIRCUIT BOARDS

Each printed circuit board shall have the following minimum quality requirements: NEMA Grade G-10 glass cloth base epoxy resin board, 1/16 inch minimum thickness, organic solder masking and gold-plated contacts. Intercomponent wiring shall be copper track, with a minimum weight of 2 ounces per square foot, with adequate cross section for current to be carried. Printed circuit design shall be such that components may be removed and replaced without permanent damage to board or tracks.

POWER

All DC power supply voltages necessary to operate the controller unit shall be developed within the controller unit.

AC power shall be supplied to the controller unit through a 3 wire power cord with a NEMA type L5-15P plug.

STANDBY POWER

A standby battery shall be provided to power the down-time accumulator and when necessary to achieve nonvolatility in the RAM during power down conditions. The battery shall have sufficient capacity for a continuous backup requirement of 8 hours for the down-time accumulator. If standby power is used to maintain RAM, it shall maintain RAM for 72 hours. Battery power shall be activated by a transfer circuit immediately upon sensing of failure in the primary power source.

The battery shall be a sealed, fast rechargeable, lead acid gel cell type suitable for standby operation. It shall be securely installed inside the Type 140 Controller unit chassis. The total weight of the standby battery shall not exceed 5 pounds. A battery charging circuit shall be provided which will fully recharge and float the battery consistent with battery manufacturer's recommendations. An indicator shall be provided which indicates the battery charge status.

CONTROL PROCESSING UNIT (CPU)

The CPU shall be a programmable microprocessor consisting of the following features:

- 8 bit parallel word, minimum
- Directly addressable to 4K x 8 bit PROM, minimum
- Directly addressable to the RAM described in this section
- Interrupt capability
- Instruction cycle time: 7 microseconds maximum

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The instruction set shall include the capabilities for data transfer; logical and arithmetic computations; accumulator rotations, increment and decrement; input/output; and shall include, but not be limited to, the following instructions:

A. Add to the contents of a register.
B. Logically "AND" with the register.
C. Take the logical compliment of a working register and store the result in a register.
D. Stop the program.
E. Add one to a working register.
F. Test the register and/or memory location and branch.
G. Conditional and unconditional Branch instructions.
H. Branch to subroutine and return instructions.
I. Rotate the contents of a register.

PROGRAMMABLE READ ONLY MEMORY (PROM)

The module containing the PROM shall provide wired sockets for 4,096 8-bit words of memory. A minimum of 2,048 8-bit words of PROM shall be provided. Each PROM chip shall be electrically programmable and erasable by exposure to ultraviolet radiation. This memory shall be nonvolatile and shall not be affected by transients resulting from power switching and external loading and unloading conditions. The PROM chips shall be the INTEL 1702A or equivalent.

Core memory is an acceptable alternative to the PROM and RAM provided all functional and environmental requirements are met.

RANDOM ACCESS MEMORY (RAM)

The RAM module shall have a minimum of 512 8-bit words and shall have fully wired empty IC sockets that permit expansion to 1024 words, when additional IC's are plugged in. The RAM shall have a read time and write time suitable to perform either function in one CPU instruction cycle. The RAM shall be alterable by word.

The RAM shall retain full memory for a minimum of 72 hours with power off. Battery backup power is permissible to retain memory.

INTERRUPT CAPABILITY

The CPU shall contain a minimum of the following Interrupt Control Signals:

A. A level requesting an interrupt to the CPU.

B. A response from the CPU allowing the external device to place its device code on the I/O bus.

POWER RESTART

When power is applied, the controller unit shall begin the execution of the program at a designated memory location.

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INPUT/OUTPUT INTERFACE

The input/output interface shall utilize negative ground true logic. Transfer of data between interfaces and working registers shall be in 8-bit word increments, minimum. The output interface shall consist of a minimum of 64 bits of buffered storage. This interface shall provide an NPN open collector output capable of driving up to +30 volts DC and sinking up to 40 milliamperes.

The input interface shall consist of a minimum of 80 bits of gated inputs from external devices at DTL/TTL levels. Each logic level input shall be turned ON (true) when the input voltage is less than 0.7 volts, shall be turned OFF (false) when the input current is less than 100 microamperes or the input voltage exceeds 2 volts, shall not place more than 24 volts or any negative voltage on an output, and shall not deliver in excess of 20 milliamperes to a short circuit to logic level common.

COMMUNICATIONS MODULE

The Communications Module shall assemble the outgoing data from the CPU from parallel to serial data characters suitable for the asynchronous modem described in Section IV. Control lines shall be included to format the transmitted messages into 1 start bit, 8 data bits and 2 stop bits.

The Communications Module shall accept the incoming asynchronous messages from the modem, removing the start and stop bits from the message, and outputting the data character to the CPU in 8 bit parallel format.

The Communication Module shall contain double character buffering for both the transmitting and receiving sides of the module. The input and output bits from the CPU required for the communications module are in addition to those required for "input/output interface".

REAL TIME CLOCK

A real time clock shall be provided to determine the time of day for data logging and control purposes. The real time clock shall operate on 60 hertz line frequency and shall cause a processor interrupt every 1/60th second.

DOWNTIME ACCUMULATOR

A downtime accumulator shall be provided which will accumulate time during power outages. Upon resumption of power, the downtime accumulator shall present an 8-bit input to the processor indicating the number of minutes of power outage with a 3% accuracy. If a power outage of more than 255 minutes occurs, the downtime accumulator

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shall indicate all ones to the processor. The downtime accumulator shall be reset to zero by an output bit under program control. The input/output bits required for the downtime accumulator are in addition to those required as input/output.

SOFTWARE

An assembler-simulator software package shall be supplied which will enable the State to:

1. Assemble State developed programs into a machine language binary code compatible with the Type 140 Controller unit supplied.

2. Simulate the Type 140 Controller unit's execution of the code.

3. Generate paper tapes in a format suitable for use with the programming system supplied.

Hardware available to perform the assembly and simulation are data General Nova 1210 minicomputers or an IBM 370, Model 168 systems computer.

TRAINING

The contractor supplying the Type 140 Controller unit shall furnish to State personnel, program, operation, and maintenance training for the controller unit, control console, and program system. Payment for training will be considered as included in the unit price paid for the Type 140 Controller units. There shall be two Program Training Classes and two Maintenance Training classes conducted at two locations within California to be selected by the State. State classroom facilities will be provided. As a result of this training, the students attending Maintenance Training must be able to load and operate diagnostic programs and to write and assemble elementary programs. Also, they must be able to troubleshoot and repair at a component level, the Type 140 Controller unit.

Students attending the Program Training Classes will have a knowledge of basic computer numbering systems and minicomputer programming (machine and assembly languages). As a result of this training these students must be able to prepare, assemble and debug a real time control program for ramp control.

Approximately ten students will attend each week-long course. Each course shall begin on a Monday morning and shall be completed within one normal work week. The instructor shall have no other duties which will interfere with his classroom duties. Each course shall contain no less than 35 hours of classroom time. The contractor shall provide all instructors and instructional material including

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DISPLAYS

The "Data Display", the "Mode Display", and the "Rate Display", as shown on the plan, shall be visible hexadecimal LED displays with integral TTL circuits to accept store, and display four-bit binary data. The characters shall be 0.27 inch high. The luminous intensity of each LED in each display shall be 50 microcandela minimum. Each character shall be LED's of a 4 x 7 matrix with latch BCH inputs, latch strobe inputs, blanking input, and left decimal point. Each display chip shall be a plug-in unit. The face of the LED shall be recessed 3/16 inch behind a 1/16 inch thick ruby red anti-reflection filter that shall be scratch, chemical, and solvent resistant.

The Control Console shall have a BCD to decimal decoder and inverter drivers, if necessary, to select the strobe latch inputs of the displays one at a time. The output of this selection device shall take the strobe latch input of the selected display to ground true logic.

THUMBWHEEL SWITCHES

The display select switch, the four input data switches, the three address switches, and the manual rate switch as shown on the plans shall be miniature hexadecimal thumbwheel switches. They shall be rated for 28 VDC at 125 milliamps and rated for over 1,000,000 detent operations. The switches shall be BCH output with cathode to switch isolation on each output pin.

INDICATOR LIGHTS

The input data indicator lights, the alarm lights, the signal lights, and the undedicated indicator lights as shown on the plans shall be incandescent lamps, visible in normal sunlight. The rated life shall be a minimum of 5,000 hours. The colors of all indicator lamps shall be as shown on the plans.

TOGGLE SWITCHES

The input data toggle switches, the undedicated toggle switches, and the manual-automatic switch all shall be SPST switches. All toggle switches shall be miniature switches rated for over 1,000,000 operations at 115 V and 0.25 amperes.

The display switch shall be a three position toggle switch with maintained and momentary contact positions. Center position shall be off, down position shall be momentary and up position shall be maintained.

The load data switch shall be guarded to prevent accidental actuation.

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The input select switch shall be a SPDT toggle switch and shall be wired so as to select either the input data thumbwheel switches or the input data toggle switches for entry into the Type 140 Controller unit.

DEVIATIONS

All proposed deviations from these console specifications must be described in detail apart from other descriptions submitted and shall be accompanied by justification based on sound engineering principles. These deviations and justifications will be considered in light of their effect on performing the functional tasks required. Price adjustment must be shown for each deviation proposed.

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SECTION VIII

PROGRAMMING SYSTEM

The programming system shall be a portable device designed for programming the type of PROM chips furnished. The programming system shall include the following features:

1. Hexadecimal keyboard for address and data entries.

2. Hexadecimal display for displaying address or data.

3. Provision to read out and display data in a PROM chip a word at a time.

4. Provision to duplicate data from one PROM chip to another. Duplication time shall be less than 1 minute.

5. Automatic comparison and verification of data between two PROM chips. The programming system shall halt on a mismatch and display the address of the mismatch and the data in both chips at that address.

6. Compartment with a built-in ultraviolet light source for erasing data in 6 or more PROM chips simultaneougly. The time required to erase PROM chips shall be less than 10 minutes. The ultraviolet light shall be switched off with an automatic timer.

   The ultraviolet light source shall be covered. It shall automatically switch off if the light is uncovered and exposed to the operators eyes.

7. The sockets that house the PROM chips during reading or writing processes shall require zero force for insertion or removal of the PROM chip.

8. Capability of reading an 8-level paper tape and writing the PROM with a program which is on the paper tape. The paper tape reading device shall be included.

   If core memory is used, the equivalent capability of programming memory shall be supplied.

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SECTION IX

ENVIRONMENTAL REQUIREMENTS AND TESTING PROCEDURES

GENERAL

The general procedures and equipment used in the evaluation of the Type 140 system including items in Section II through VIII of these specifications are only a minimum guideline and should not limit the testing and inspection which will properly assure the compliance of the system with these specifications.

These test procedures are not only for use by the State testing agency, but for the manufacturer of the equipment who shall certify that he has conducted inspection and testing in accordance with these specifications.

INSPECTION

A visual and physical inspection shall include mechanical dimensional and assembly conformance of all parts of these specifications which can be checked visually or manually with simple measuring devices. Workmanship shall be in accordance with the highest industry standards.

ENVIRONMENTAL

All compontents in this system shall properly operate under the following conditions:

Humidity	0 to 90% at 40° C
Powerline	117±13 VAC, 60±3 Hertz
Transient	Calif. 667A
Shock	Mil.-std.-810 Method 516.1
Vibration	Mil.-std.-810 Method 514.1 equipment class 6

Items under Sections II, III, IV, VI and VII of these specifications shall operate in an ambient environment of - 18° C to + 60° C and comply with the requirements of UL Bulletin of Research No. 23 "Rain Tests of Electrical Equipment". Items under Section V and VIII of these specifications shall operate in an ambient environment of 25° C. The ambient environment is defined as the temperature and humidity measured outside the cabinet.

DIAGNOSTIC PROGRAM

A diagnostic program shall be written by the manufacturer of the Type 140 Controller unit which will demonstrate the proper operation

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of all of the inputs, outputs, controls and indicators in the controller and the Control Console. The program shall demonstrate the read function of each PROM chip and socket and the write-read function of each RAM chip and socket. This program shall be written in the language of the processor which is supplied and shall be resident in each Type 140 controller when delivered to the State for testing.

A flow chart and listing of the diagnostic routine shall be furnished with each Type 140 controller unit.

TESTING

All tests shall be conducted at three temperatures - 18° C, 25° C, and 60° C for all items except V and VIII. The complete cabinet with all components shall soak at the test temperature for at least 12 hours before power is applied. The diagnostic program shall be resident in the controller and all input-output functions shall demonstrate EIR operation.

The diagnostic program shall be run at all three temperatures at the line voltage levels of 105 VAC and 130 VAC. The power line transient test shall be run at the three temperatures.

All items shall be tested and a passing or failing indication noted. A log of items which do not comply with specifications shall be kept throughout the testing period.

MANUFACTURERS TESTING CERTIFICATION

The manufacturer shall supply with each item a full test report of the quality control and final test conducted on each unit. The test report shall indicate the tester and shall be signed by a responsible manager.

A minimum of 10% or two units, whichever is greater, shall be tested at -18° C and at 60° C. All units shall be fully tested at 25° C.

REJECTION

Only complete shipments with all units ready for test shall be shippped to the State testing facilities. If a partial shipment is received by the State, that shipment will be automatically rejected and a subsequent testing cost on that shipment shall be paid for by the manufacturer and shall be deducted from payment due to him.

The State will test all units in a shipment and will reject the entire shipment if any unit fails to comply with these specifications due to defects or deviations. All subsequent testing on that shipment shall be at the manufacturer's expense.

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TRAFFIC ENGINEER
REGISTERED CIVIL ENGINEER NO _____
DATE APPROVED _____

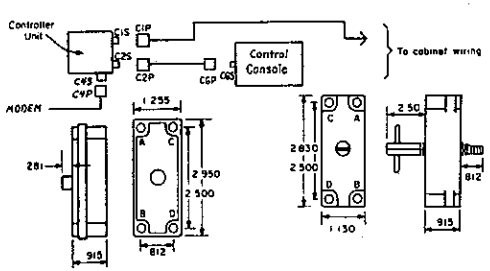
CONNECTOR C1P AND C1S

PIN	SOURCE	FUNCTION	PIN	SOURCE	FUNCTION	PIN	SOURCE	FUNCTION	PIN	SOURCE	FUNCTION
1	DC Grd	DC Ground	27	04-1	NC	53	12-7	TB1-1	79	16-5	NC
2	01-1	LD SW1-Red	28	04-2	NC	54	12-8	TB1-2	80	16-6	NC
3	01-2	LD SW1-Grn	29	04-3	NC	55	13-1	TB1-3	81	16-7	NC
4	01-3	LD SW2-Red	30	04-4	NC	56	13-2	TB1-4	82	16-8	NC
5	01-4	LD SW2-Yel	31	04-5	NC	57	13-3	TB1-5	83	06-1	NC
6	01-5	LD SW2-Grn	32	04-6	NC	58	13-4	TB1-6	84	06-2	NC
7	01-6	LD SW3-Red	33	04-7	NC	59	13-5	TB1-7	85	06-3	NC
8	01-7	LD SW3-Yel	34	04-8	NC	60	13-6	TB1-8	86	06-4	NC
9	01-8	LD SW3-Grn	35	05-1	NC	61	13-7	TB1-9	87	06-5	NC
10	02-1	NC	36	05-2	NC	62	13-8	TB1-10	88	06-6	NC
11	02-2	NC	37	05-3	LD SW1-Yel	63	14-5	TB1-11	89	06-7	NC
12	02-3	NC	38	05-4	NC	64	14-6	TB1-12	90	06-8	NC
13	02-4	NC	39	11-1	Detector 1	65	14-7	Pol/Ent PT SW	91	07-1	NC
14	DC Grd	DC Grd-DC RK	40	11-2	Detector 2	66	14-8	Pol Lights SW	92	DC Grd	Output Grd
15	02-5	NC	41	11-3	Detector 3	67	15-1	NC	93	07-2	NC
16	02-6	NC	42	11-4	Detector 4	68	15-2	NC	94	07-3	NC
17	02-7	NC	43	11-5	Detector 5	69	15-3	NC	95	07-4	NC
18	02-8	NC	44	11-6	Detector 6	70	15-4	NC	96	07-5	NC
19	03-1	NC	45	11-7	Detector 7	71	15-5	NC	97	07-6	NC
20	03-2	NC	46	11-8	Detector 8	72	15-6	NC	98	07-7	NC
21	03-3	NC	47	12-1	Detector 9	73	15-7	NC	99	07-8	NC
22	03-4	NC	48	12-2	Detector 10	74	15-8	NC	100	05-5	NC
23	03-5	NC	49	12-3	Detector 11	75	16-1	NC	101	05-6	NC
24	03-6	NC	50	12-4	Detector 12	76	16-2	NC	102	05-7	NC
25	03-7	NC	51	12-5	Detector 13	77	16-3	NC	103	05-8	NC
26	03-8	NC	52	12-6	Detector 14	78	16-4	NC	104	DC Grd	Input Grd

CONNECTOR C2P AND C2S

PIN	SOURCE	FUNCTION	PIN	SOURCE	FUNCTION	PIN	SOURCE	FUNCTION	PIN	SOURCE	FUNCTION
1	DC Grd	DC Ground	27	04-1	NC	53	07-7	NC	79	18-1	In Data 100
2	01-1	NC	28	04-2	NC	54	07-8	NC	80	18-2	In Data 200
3	01-2	NC	29	04-3	NC	55	14-1	Man Rate 1	81	18-3	In Data 400
4	01-3	NC	30	04-4	NC	56	14-2	Man Rate 2	82	18-4	In Data 800
5	01-4	NC	31	04-5	NC	57	14-3	Man Rate 4	83	18-5	In Data 1000
6	01-5	NC	32	04-6	NC	58	14-4	Man Rate 8	84	18-6	In Data 2000
7	01-6	Red Sig Lt	33	04-7	NC	59	14-5	Display SW	85	18-7	In Data 4000
8	01-7	Yel Sig Lt	34	04-8	NC	60	14-6	Input SW	86	18-8	In Data 8000
9	01-8	Grn Sig Lt	35	05-1	Alarm Lite 1	61	14-7	Man-Auto SW	87	19-1	Address 1
10	02-1	In Data Lt 1	36	05-2	Alarm Lite 2	62	14-8	NC	88	19-2	Address 2
11	02-2	In Data Lt 2	37	05-3	Alarm Lite 3	63	15-1	Spare SW 1	89	19-3	Address 4
12	02-3	In Data Lt 3	38	05-4	Alarm Lite 4	64	15-2	Spare SW 2	90	19-4	Address 8
13	02-4	In Data Lt 4	39	06-1	Blkg Digit 1	65	15-3	Spare SW 3	91	19-5	Address 10
14	DC Grd	DC Ground	40	06-2	Blkg Digit 3	66	15-4	Spare SW 4	92	DC Grd	DC Ground
15	02-5	In Data Lt 5	41	06-3	Blkg Digit 2	67	15-5	Spare SW 5	93	19-6	Address 20
16	02-6	In Data Lt 6	42	06-4	Decimal Pt.	68	15-6	Spare SW 6	94	19-7	Address 40
17	02-7	In Data Lt 7	43	06-5	Dp Dev Sel 1	69	15-7	Spare SW 7	95	19-8	Address 80
18	02-8	In Data Lt 8	44	06-6	Dp Dev Sel 2	70	15-8	Spare SW 8	96	110-1	Address 100
19	03-1	Spare Lt 1	45	06-7	Dp Dev Sel 4	71	17-1	In Data 1	97	110-2	Address 200
20	03-2	Spare Lt 2	46	06-8	Dp Dev Sel 8	72	17-2	In Data 2	98	110-3	Address 400
21	03-3	Spare Lt 3	47	07-1	Display 1	73	17-3	In Data 4	99	110-4	Address 800
22	03-4	Spare Lt 4	48	07-2	Display 2	74	17-4	In Data 8	100	110-5	Display Sel 1
23	03-5	Spare Lt 5	49	07-3	Display 4	75	17-5	In Data 10	101	110-6	Display Sel 2
24	03-6	Spare Lt 6	50	07-4	Display 8	76	17-6	In Data 20	102	110-7	Display Sel 4
25	03-7	Spare Lt 7	51	07-5	NC	77	17-7	In Data 40	103	110-8	Display Sel 8
26	03-8	Spare Lt 8	52	07-6	NC	78	17-8	In Data 80	104	DC Grd	DC Ground

NC - NOT CONNECTED
01-1 - OUTPUT DEVICE 1 BIT 1
I1-8 - INPUT DEVICE 1 BIT 8
Blanking Digit 4 - MOST SIGNIFICANT DIGIT
TB1 - TERMINAL BLOCK

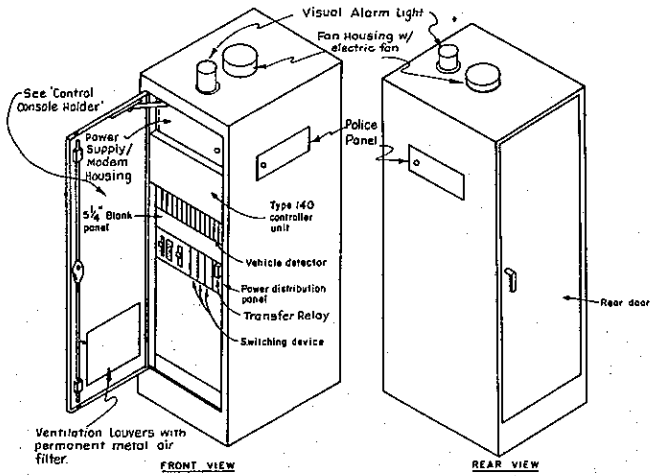


Corner Guides
C1S - pins A and D, sockets B and C
C2S - pin C socket A, B and D

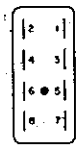
CONNECTORS C1S, C2S

Corner Guides
C1P - pins B and C, sockets A and D
C2P - pins A, B and D, socket C

CONNECTORS C1P, C2P

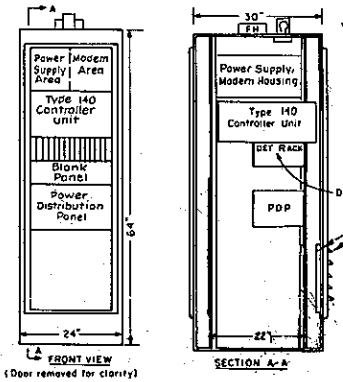


CABINET
No Scale
Equipment Layout

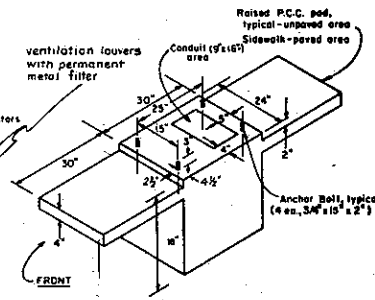


PIN NO.	FUNCTION
1	Coil
2	Coil
3	N.C. Circuit # 1
4	N.C. Circuit # 2
5	Common Circuit # 1
6	Common Circuit # 2
7	N.O. Circuit # 1
8	N.O. Circuit # 2

TRANSFER RELAY SOCKET
No Scale

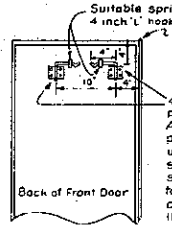


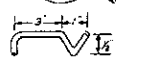
CABINET DETAILS
No Scale
Dimension tolerance ±1/8"



FOUNDATION DETAILS
No Scale

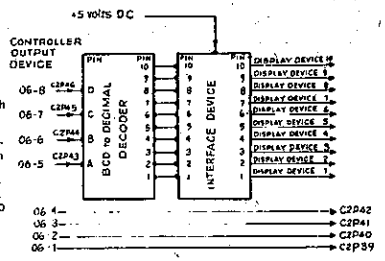
CONTROL CONSOLE HOLDER
No Scale



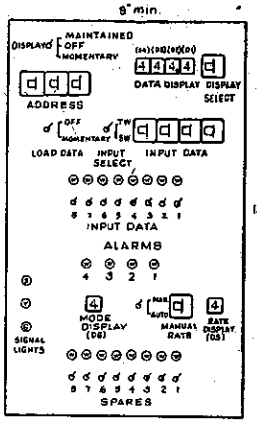


L HOOK ARM DETAIL

BCD TO DECIMAL DECODER DETAIL
No Scale

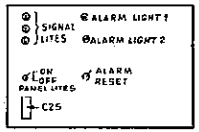


Interface shall utilize negative ground true logic to activate the desired display device holding all other devices at + 5 v DC.



CONTROL CONSOLE

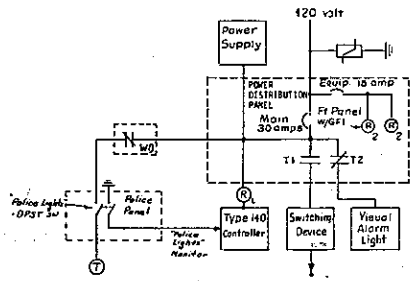
LEGEND
- White Lens (G-Green, Y-Yellow, R-Red)
- Toggle Switch
- Thumbwheel Switch
- Display Readout
D4 - Display Device 4



TYPE 140 CONTROLLER UNIT FRONT PANEL
No Scale

CONNECTOR C3
(Edge Connector CPU to Front Panel)

01-6	08-1	I5-4
01-7	08-2	I5-5
01-8	08-3	I5-6
05-1	08-4	I5-7
05-2	08-5	I5-8
05-3	08-6	I6-1
05-4	08-7	I6-2
07-5	08-8	I6-3
07-6	I5-1	I6-4
07-7	I6-2	I6-5
07-8	I5-3	I6-6
		I6-7
		I6-8



RAMP CABINET ONE LINE DIAGRAM

LEGEND
- Circuit Breaker
- Receptacle, Duplex
- Receptacle, Locking
- Relay, Coil
- Relay, Contact N.O.
- Relay, Contact N.C.
- Surge Arrestor
- Switch
- Watchdog Monitor

TECHNICAL PLAN

TYPE 140 CONTROLLER
TYPICAL DETAILS

12 - -74

SES-35 A

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